Tutorial Proposal on "Error Resilient Digital and Analog Circuit Design"

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- Parameter variations/Reliability considerations and the need for error resiliency in scaled technology
- Modeling parameter variations – inter die and intra-die variations
- Modeling of reliability degradations – BTI (Bias temperature Instability), HCI (Hot Electron Injection), TDDB (time Dependent Dielectric Breakdown)
- Error resilient digital system design (better than worst case design)
    - Design time and run time techniques for logic and memories
        - Logic
            - Sizing, pipeline imbalancing
            - Sense and correct with adaptive body biasing, adaptive beta-ratio modulation for low voltage designs
            - Critical Path Isolation with Timing Adaptivity (CRISTA)
            - Razor design approach
            - Algorithmic Noise Tolerance (ANT)
            - Adaptive Latency Microarchitectures
            - Adaptive Latency and Voltage Interpolation
        - DSP Systems
            - Process tolerance and low voltage design using adaptive quality modulation
                - Digital Filters, DCT, Motion Estimation etc.
        - Memories
            - Memory failures under parameter variations
            - Bit-cell design for low Vmin
                - 6T, 8T, 10T and sizing
            - Array and architecture level techniques for error resiliency
            - Error resilient register files
    - Design challenges under variation with analog circuits
        - Analog and RF design in scaled technologies, challenges in radio design
        - Techniques to overcome variations
        - Low-power approaches from device to architecture

Bio:

Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He was with the Semiconductor Process and Design Center of Texas Instruments, Dallas, where he worked on FPGA architecture development and low-power circuit design. He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently a Professor and holds the Roscoe H. George Chair of Electrical & Computer Engineering. His research interests include Spintronics, VLSI design/CAD for nano-scale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, VLSI testing and verification, and reconfigurable computing. Dr. Roy has published more than 500 papers in refereed journals and

conferences, holds 15 patents, graduated 50 PhD students, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill).

Dr. Roy received the National Science Foundation Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, Purdue College of Engineering Research Excellence Award, Humboldt Research Award in 2010, and best paper awards at 1997 International Test Conference, IEEE 2000 International Symposium on Quality of IC Design, 2003 IEEE Latin American Test Workshop, 2003 IEEE Nano, 2004 IEEE International Conference on Computer Design, 2006 IEEE/ACM International Symposium on Low Power Electronics & Design, and 2005 IEEE Circuits and system society Outstanding Young Author Award (Chris Kim), 2006 IEEE Transactions on VLSI Systems best paper award. Dr. Roy is Purdue University Faculty Scholar. He was a Research Visionary Board Member of Motorola Labs (2002) and held the M.K. Gandhi Distinguished Visiting faculty at Indian Institute of Technology (Bombay). He has been in the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems, and IEEE Transactions on VLSI Systems. He was Guest Editor for Special Issue on Low-Power VLSI in the IEEE Design and Test (1994) and IEEE Transactions on VLSI Systems (June 2000), IEE Proceedings -- Computers and Digital Techniques (July 2002). Dr. Roy is a fellow of IEEE.

Byunghoo Jung received the B.S. degree from Yonsei University, Korea, in 1990, the M.S. degree from KAIST, Korea, in 1992, and the Ph.D. degree from the University of Minnesota, Twin Cities, in 2005. From 1992 to 1999, he was with Samsung Electronics, Korea, where he was involved in the design of video signal driver circuits for flat panel displays. Following receipt of his PhD in January 2005, he was with Qualcomm in San Diego as a Senior RF IC Design Engineer until he joined the School of Electrical and Computer Engineering at Purdue University as an Assistant Professor in August 2005. His research interests include analog, RF, and mixed-signal circuit design for wireless and wireline communications and bio-medical systems. He is the first place winner of the 2002-2003 SRC SiGe BiCMOS Design Challenge (as a lead designer) and the 2007-2008 SRC/SIA IC Design Challenge (as a lead faculty), and holds 10 US patents. He has been serving as a Co-Chair of *the DAC/ISSCC Student Design Contest* (SDC) since October 2006, as an Associate Editor of *the IEEE Transactions on VLSI Systems* since January 2009, and as a member of the Analog Signal Processing Technical Program Committee (ASPTPC) in *the IEEE Circuits and System Society* since May 2006.