1. TITLE AND SUMMARY

Design methodology and techniques in production low-power SOC designs

SUMMARY

Power has become critical metric and key differentiator in sub-65nm SOC designs, due to growing power density driven by technology scaling and chip integration. This tutorial provides overview of the low-power design methodologies and techniques in production SOC design perspective, emphasizing on the real design considerations and impact on chip success. We shall discuss pros and cons of the methods and techniques considering impacts on chip design schedule, yield, and overall power-performance target. We shall also provide design guidance and recommendations in various design steps and decision making points, based on our years of successful experience in production low-power SOC designs.

This tutorial is organized in two parts. In the first part, we shall overview power related challenges in sub-60nm SOC design and state-of-the-art techniques to reduce chip power. We shall give a holistic view from chip level to system and application levels. Practical industrial examples will be used to show how power savings can be achieved in modern SoC, processors and computer systems. In the second part, we shall describe production low-power design methodology and techniques particularly the power-gating and the voltage/frequency scaling which are the two advanced power reduction methods used effectively in sub-65nm production low-power designs. We shall explain when, where and how these methods and techniques are applied to a chip according to the design goals and time-to-market requirement. We shall also cover production low-power design methodology and flow with UPF power intent and unified design environment.

2. PRESENTERS

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3. TARGETED AUDIENCE AND PREREQUISITES

engineers, researchers and project managers.
General understanding of SOC design

4. KEYWORDS

VLSI

5. DETAILED TUTORIAL PROGRAM

Part 1.

- Introduction
  - History of IC design challenges under different constraints
  - Power vs. Energy
  - Static and dynamic power
- Factors driving design for low power – electrical, physical, environmental and economic issues
  - Growing power and cooling cost
  - Power consumption in data centers
  - Physical issues: Heat dissipation, mechanical stress, electromigration, etc.
  - Electrical issues: Voltage drop, noise, etc.
- System view
  - Off-chip power dissipation contributors
  - Example: Power consumption in a high-end server
  - Power, packaging, cooling
- Overview of power reduction techniques
  - Techniques and their tradeoffs
  - Diminishing returns through levels of abstraction
  - Design techniques: Gate level optimization, multi-VT, clock gating, power gating, multiple voltage domains
  - Technological remedies: e.g. strained Si, Hi-K/metal gates, MuGFETs etc.
- Power management on system and chip level – example: POWER™ processor architecture
  - Conceptual Topology (EnergyScale™ architecture, thermal sensors, activity counters, critical path monitor, etc.)
  - Power/Performance optimization – power/thermal capping, performance-sensitive power savings, throttling, idle modes, dynamic voltage/frequency scaling
  - Feasibility for non-processor SOCs – example: power saving in I/O hub chips
- New ideas for power saving
  - Glitch power – the unknown factor
  - A system and method for glitch power avoidance

Part 2.

- Voltage/frequency scaling (10 m)
  - task/performance profiling based DVFS – overview, pros and cons
  - adaptive DVFS – overview, pros and cons
  - app and PTV based VFS - overview, pros and cons
  - production design considerations and recommendations

- Power-gating design (40 m)
    - Principle, system, elements, management and sequence
    - Retention strategies and techniques – ext vs. internal retention, dual and single control flops, pulse-triggered retention flop, retention rams
    - Tradeoffs – area, complexity, risk, schedule, performance
    - Theoretic vs. real power saving
    - strategies for production design - decision points and criteria
- Overview of low-power SOC implementation flow (30 m)
    - Domain partitioning – production design considerations and criteria (function locality, operability, performance target, size etc), fplan-aware
    - Power management strategy – things to watch (pending, running, interrupt), central vs hierarchical control, input vs output isolations, retentions, low-power IPs, sleep/wakeup sequence
    - Switched power network – ring vs distributed, optimal switch insertion, switch hookup, ao- and switched-vdd grids. Production design considerations
    - Ao-tap insertion and ao-vdd supply challenges in tapless production design – considerations
    - Domain-aware logical/physical synthesis – ao-synthesis, isolation and level shifting integrity, cts, routing
- Overview of power intent definitions through UPF (5 m)
    - - power domain, supplies, .. – power intents for DV and implementation - examples
- Overview of production low-power design environment (5 m)
    - - address flow challenges – many details in the implementation could go wrong by human mistakes, examples …

6. HALF DAY

7. BIBLIOGRAPHY

1. (book) David Flynn, Michael Keating, Robert Aitken, Alan Gibbons and Kaijian Shi , “Low Power Methodology Manual for System-on-Chip Design”, Springer, 2007
2. Kaijian Shi, Zhian Lin, Yi-min Jiang, Lin Yuan “Simultaneous Sleep Transistor Insertion and Power Network Synthesis for Industrial Power Gating Designs”, Journal of Computer, Academy Publisher Vol. 3 No.3 March, 2008
3. Kaijian Shi and David Flynn, “Power Gating Design Tradeoffs And Considerations In Production Low-power Designs”, Proc. IEC DesignCon, Feb., 2009
4. Kaijian Shi, “Area and Power-Delay Efficient State Retention Pulse-triggered Flip-flops with Scan and Reset Capabilities”, Proc. International Conference of Computer Designs (ICCD), Oct.,. 2008
5. Kaijian Shi, Jingsong Li, “A Wakeup Rush Current and Charge-up Time Analysis Method for Programmable Power-Gating Designs”, IEEE SoC Conference, Sep. 2007
6. Kaijian Shi, Julio Hernandez, Joe Geisler, “IR-drop analysis of a complex power-gating design”, Proc. SNUG-Boston, 2007
7. Kaijian Shi, Zhian Lin, Yi-min Jiang, “A Power Network Synthesis Method for Industrial Power Gating Designs”, Proc. IEEE Int. Symposium on Quality Electronic Design (ISQED), March, 2007
8. Kaijian Shi and David Howard, “Sleep Transistor Design and Implementation – Simple Concepts Yet Challenges To Be Optimum”, Proc.. IEEE VLSI-DAT, April, 2006
9. David Howard & Kaijian Shi, “Power-On Current Control In Sleep Transistor Implementations”, Proc.. IEEE VLSI-DAT, 2006
10. Kaijian Shi and Jason Binney, “Low Power Design Methodologies and Optimization for Sub-90nm ASIC”, Proc.

DesignCon, Feb. 2005

11. Kaijian Shi and Jason Binney, “Design Optimization Methodologies for Low-Leakage Power Designs in Sub-90nm Technology”, Proc. Euro DesignCon, Oct. 2004
12. Kaijian Shi, James Song et. al “Hierarchical Timing Closure Methodology for OMAP™: An Open Multimedia Application Platform”, Proc. IEEE Conference on ASIC (ASCION2003), Oct., 2003
13. James Song, Kaijian Shi, et. al. “A Low Power Open Multimedia Application Platform for 3G Wireless”, Proc. IEEE International SOC Conference, Portland, Sep., 2003
14. Kaijian Shi, James Song et. al. “Clock distribution and balancing Methodology for a large and complex ASIC”, Proc. IEC DesignCon-East, Boston, Jun., 2003 (invited paper)
15. Kaijian Shi and Craig Godwin, “Hybrid Hierarchical Timing Closure Methodology for a High Performance and Low Power DSP”, Proc. ACM/IEEE Design Automation Conference (**DAC**), June., 2003
16. Lei Wang, Markus Olbrich, Thomas Büchner, Markus Bühler, Erich Barke, “Fast Dynamic Power Estimation Considering Glitch Filtering,“ Proc. IEEE International SOC Conference, pp.361-4, Belfast, Northern Ireland, UK, Sept. 2009, ISBN 978-1-4244-5220-0
17. Ramalingam Sridhar, Thomas Büchner, Ram K. Krishnamurthy (Editors), "12th Annual IEEE International ASIC/SOC Conference - Digest of Technical Papers" Washington, DC, 1999, IEEE Catalog No. 99TH8454, ISBN: 0-7803-5632-2
18. Mark E. Schrader, Ramalingam Sridhar, Thomas Büchner, Paul P.K. Lee (Editors), "Proceedings Eleventh Annual IEEE International ASIC Conference," Rochester, NY, 1998, IEEE Catalog No. 98TH8372, ISBN: 0-7803-4980-6

8. TUTORIAL SLIDES

9. SHORT BIO

Kaijian Shi is Principal Consultant in Synopsys Professional Services Group since 1999, specializing in low-power design methodology and implementation. He has worked as a consultant on more than 11 leading-edge commercial low-power designs all taped out successfully. Dr. Shi is one of the people pioneering the low-power implementation methodology developments and chip design in EDA and semiconductor industry. He has been a key contributor to the development of the advanced low-power production design flow in a leading semiconductor company which he has been consulting for. Dr. Shi co-authored the book “Low Power Methodology Manual for System-on-Chip Design” and has published 53 papers in journals and international conferences. He holds a Ph.D. degree from University of Kent at Canterbury, UK since 1994. Dr. Shi was Chairman of IEEE Dallas Section in 2006 and Chairman of IEEE Circuits and System Society Dallas Chapter in 2004. He was Workshop chair and then publicity chair of IEEE SoC Conference 2008-2010 and program committee members of IEEE ISVLSI (2006-2008) and DesignCon since 2003.

Thomas Buechner is Advisory Engineer at IBM Research & Development Lab in Boeblingen, Germany, since 1994, where he is currently responsible for the design of power management units for IBM’s next generation POWER™ processors. Before that he has been involved in the development of many chips for high-end servers, from I/O hubs to complex SoCs. From 2007-2009 he led a workgroup to increase the power efficiency of server I/O hardware.
He holds a Ph.D. degree from Stuttgart University since 1996. From 1989 to 1993 he was a Research Engineer at Institute for Microelectronics Stuttgart, Germany (IMS-Chips). He has published numerous papers at international conferences and holds several patents in the area of chip design and power reduction.
Dr. Buechner has been involved in IEEE ASIC, IEEE ASIC/SOC and IEEE SoC Conference (SOCC) since 1995,

where he held several positions, including Program Chair, General Chair, and Steering Committee Chair. He is General Chair of IEEE SOCC 2010 and acted as reviewer for numerous conferences including DAC, DATE, RAW, ASIC, ASIC-SOC, SOCC, DCIS, and ISVLSI.