3D Integrated Circuit Design

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Abstract
Despite generation upon generation of technology scaling, computer chips have remained essentially two-dimensional (2D). Improvements in the on-chip wire delay, and in the maximum number of inputs and outputs per chip have not been able to keep up with transistor performance growth, and it has become progressively harder to hide the discrepancy. In addition, the complexities of lithography beyond the 32 nm node threaten the traditional performance and cost scaling paradigms. In contrast with these conventional 2D circuits, 3D integrated circuits offer a new paradigm that builds multiple tiers of active devices stacked above each other. Recent advances in process technology have brought 3D technology to the point where it is feasible and practical, and it has raised widespread interest in the chip industry. The move to 3D allows numerous benefits over 2D, such as reduced interconnect lengths, improved computation per unit volume, and the possibility of integrating heterogeneous systems. However, the paradigm requires a significant change from contemporary design methodologies, since an optimal 3D chip design has very different characteristics from an optimal 2D chip design. The goal of this tutorial is to provide an overview of the technology, the corresponding design challenges, and existing solutions to overcome these challenges.

3D chip technologies come in a number of flavors that are expected to enable the extension of CMOS performance. Designing in 3D forces the industry to look at formerly-two-dimensional integration issues quite differently, and requires the re-fitting of multiple existing EDA capabilities. We begin with an overview of the motivation for 3D, process steps, and delve into the design issues in detail.

We then address how the technology can be used to provide significant performance benefits: up to now 3DIC technologies, through silicon vias (TSV), and bonding techniques, have mainly been exploited in view of their potential for miniaturization. However, the open question is how to exploit 3DIC for reasons beyond just size and weight. It is becoming clear that if the system is re-architected to explicitly account for 3D IC technology, advantages can be gained in performance, power consumption, and cost. However, complicating factors that must be dealt with include partitioning, design management, thermal design, and manufacturing test.

A key part of the 3D solution lies in the development of EDA solutions to address such 3D-specific issues, and the next part of the tutorial overviews the specific role for new computer-aided design (CAD) tools that can solve problems related to building designs in 3D: specifically, 3D physical design, thermal management, and power delivery. We will also discuss how one can extend the existing 2D design flows to adapt to 3D as opposed to inventing new flows. Design flow steps unique to 3D will also be described.

Since testing remains a major obstacle that hinders the adoption of 3D integration, test challenges for 3D SICs must be addressed before high-volume production of 3D SICs can be practical. This part of the tutorial will present recent breakthroughs in test technology that promise higher levels of silicon integration, fewer defect escapes, and commercial exploitation. The presentation will be divided into three parts:

1. Test content development: The presenters will highlight defects that are unique to 3D processing steps of alignment, stacking, thinning, and through silicon via (TSV) insertion. Test methods will be described to target edge effects in wafer bonding, thermal expansion of vias, microbumps, and C4 pads, TSV misalignment, and TSV underfill/overfill. Both pre-bond and post-bond test methods will be covered.
2. Test delivery optimization: This part of the tutorial will highlight the DFT infrastructure needed for pre-bond test and post-bond test. The design of die wrappers, test modes, and test access paths will be presented. Stack testing requires the layers to be wrapped to allow different modes such as bypass (for providing access to other layers), TSV test, and die-internal test. Therefore, wrapper design must go beyond the IEEE 1500 Standard. Optimization and test scheduling techniques will be described for stack test and managing multiple test insertions.
3. Cost analysis: A cost-analysis framework will be presented to unify design, manufacturing, and test aspects of 3D SIC cost. Test cost, wafer cost, yield, bonding cost, etc. interact with each other, and tradeoffs are needed to minimize overall cost.

Finally, the tutorial will address architectural issues in 3D design. Design space exploration at the architectural level is essential to fully take advantage of the 3D integration technologies and to build high performance microprocessors. In this tutorial, we will discuss fine-granularity and coarse-granularity processor design options, and present various novel architecture designs enabled by 3D integration, leveraging the benefits of faster and high-bandwidth communication to stacked layer, as well as the heterogeneous integration capability.

Topical Outline

3D technology

- Technological motivation for 3DIC technology
- Technology alternatives and features from a designers perspective
- ASIC sub-system partitioning alternatives for 3DIC
- Chip-package codesign for 3DIC
- Executing 3D designs
- Future challenges in 3DIC

Architecture for 3DIC Processors

- Technology Scaling Trends
- Tera-scale computing
- Implications to interconnects
- 3D die/wafer stacking considerations
- 3D challenges – test, EDA, thermal

CAD Solutions for 3D Systems

- CAD challenges for 3D systems
- 3D-specific challenges
- A 3D design flow
- Thermal issues in 3D design
- 3D power delivery
- Leveraging 3D for optimized communication

Test Solutions for 3D Systems

- Test Content development
- Test delivery optimization
- Cost analysis