Future of Analog Design and Upcoming Challenges in Nanometer CMOS

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VLSI Design 2010

Outline

- **Introduction**
- Logic processing trends
- Analog design trends
- Analog design challenge
- Approaches
- Conclusion

Introduction

- This talk will focus on analog design on digital processes
  - Small geometries
  - Low voltages
  - Integration with logic
- Processes optimized for analog circuits are a different problem

Introduction (cont)

- Intel view:
  - Don't get in the way of digital scaling
  - Transistor count doubles every 24 months
  - Don't violate the Law!
- Alternative view
  - Logic processes are leading the way to smaller geometries
    - They provide the first look at the design of analog circuits at these feature sizes

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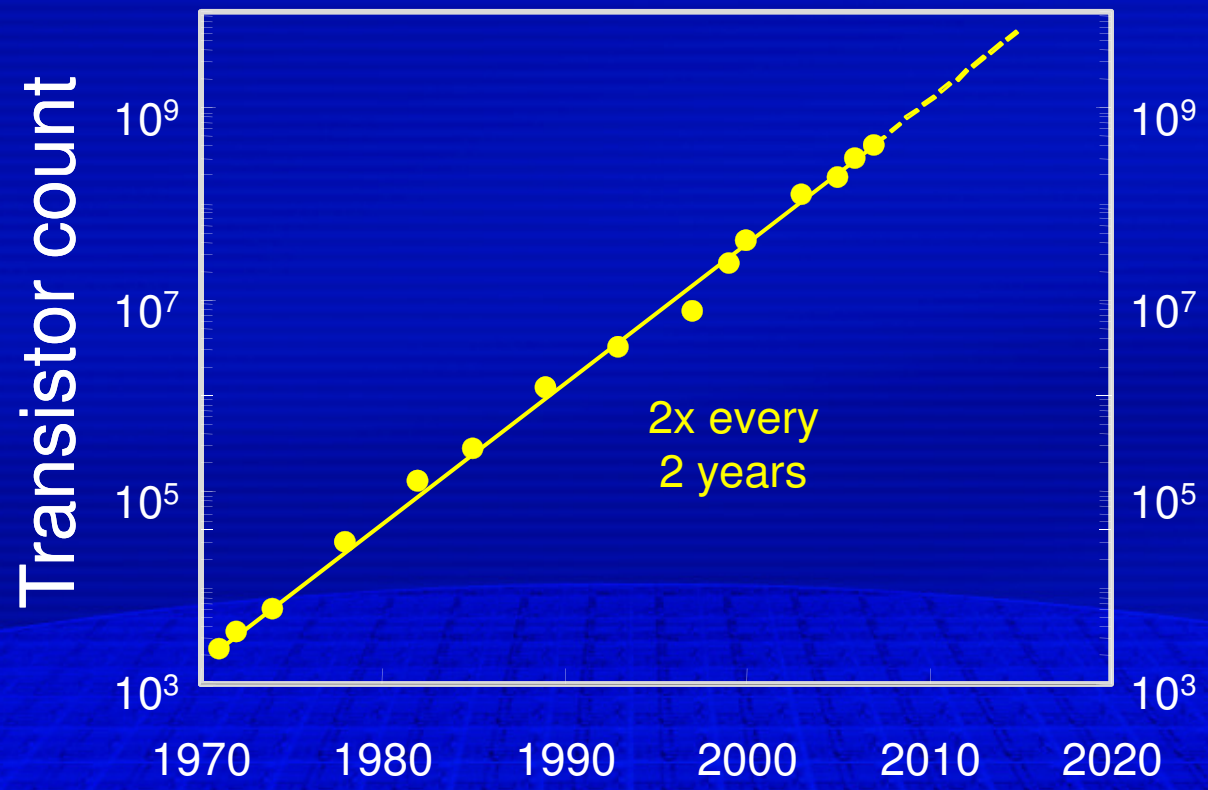
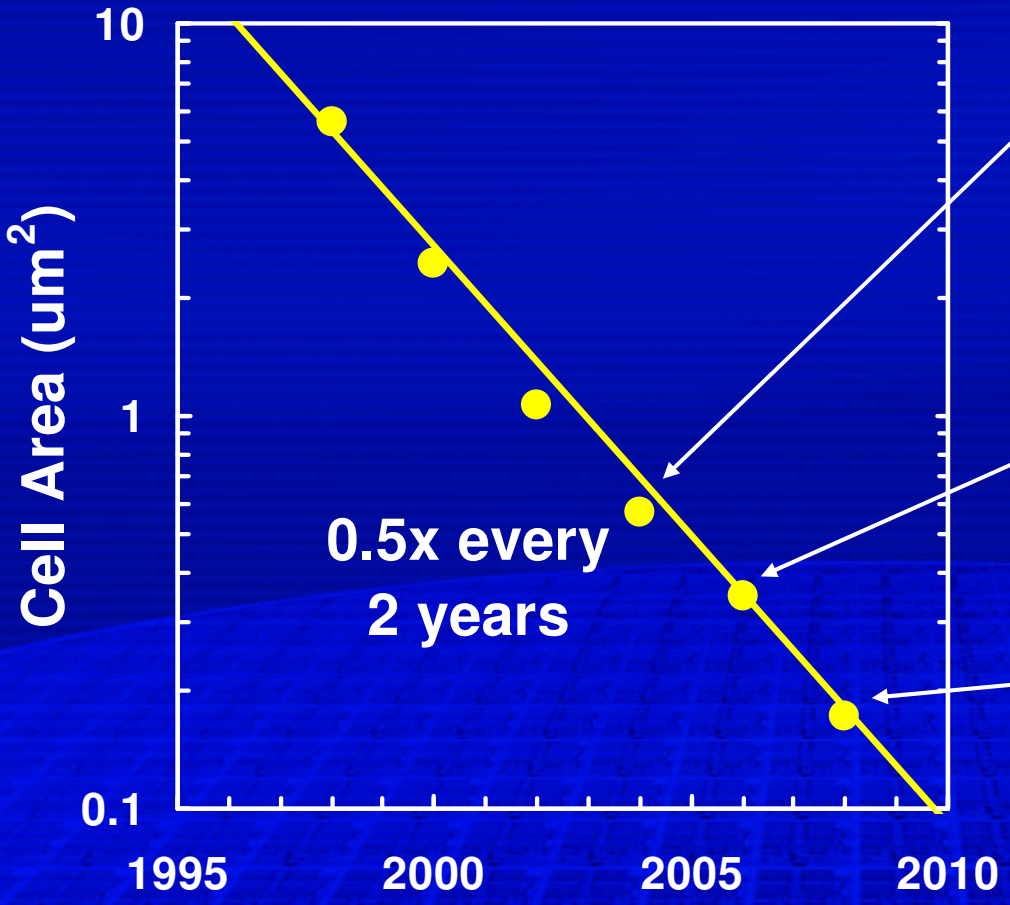
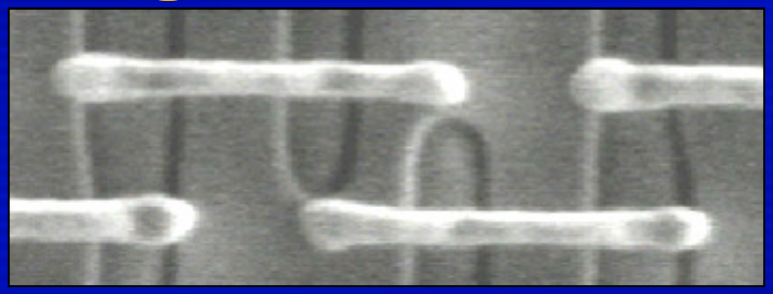
Logic Processing Trends



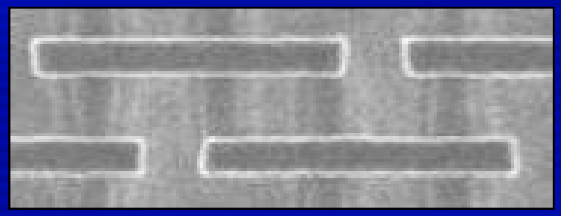
- **Performance and functionality continue to improve with increased transistor count**

SRAM Scaling

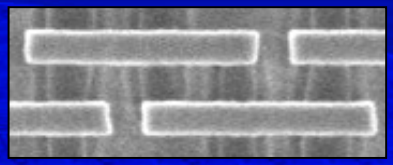




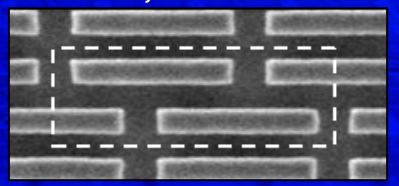
65 nm, 0.570 um²



45 nm, 0.346 um²



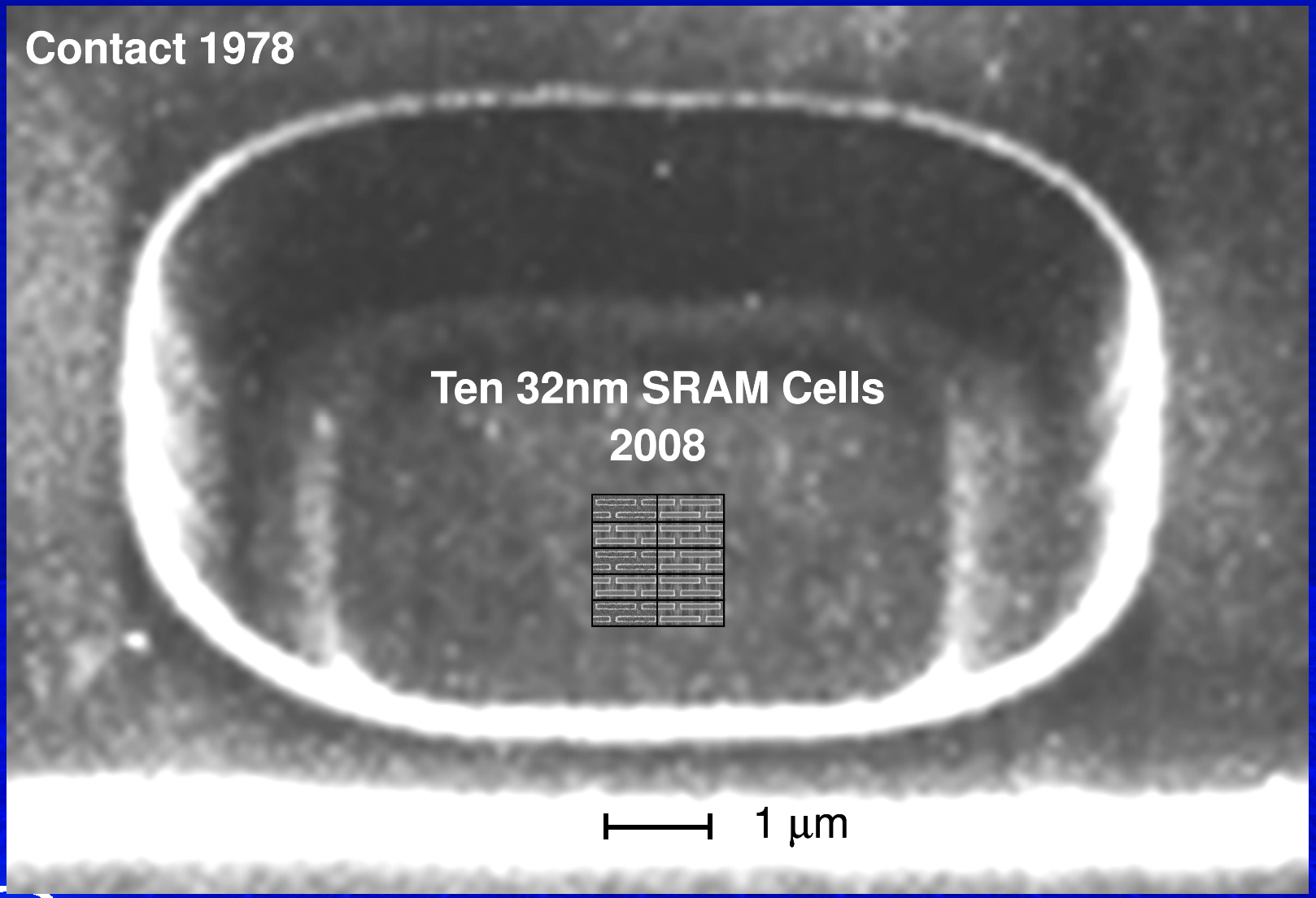
32 nm, 0.171 um²



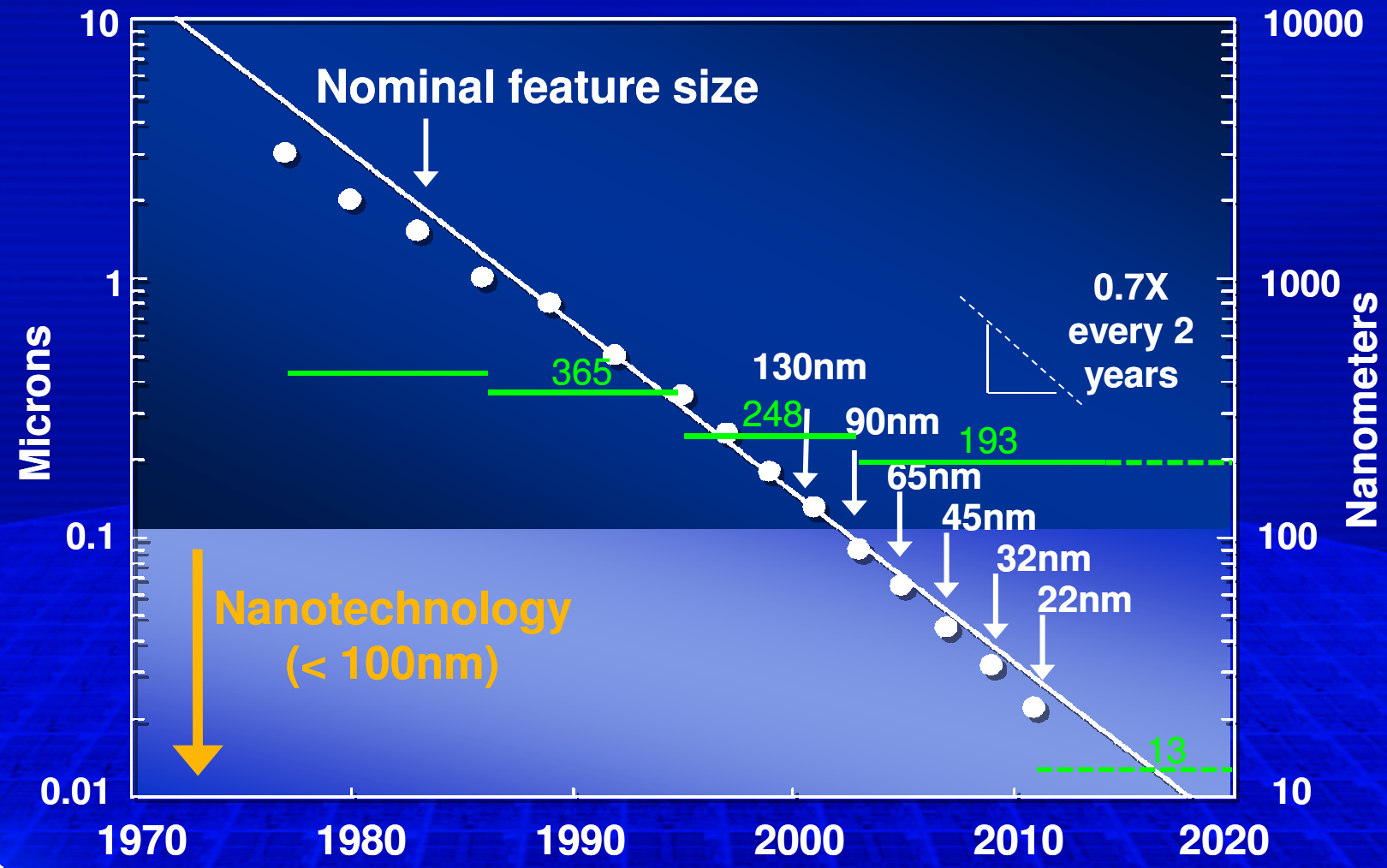
22 nm, 0.092 um²

Mark Bohr: IDF 2009

30 Years of Scaling

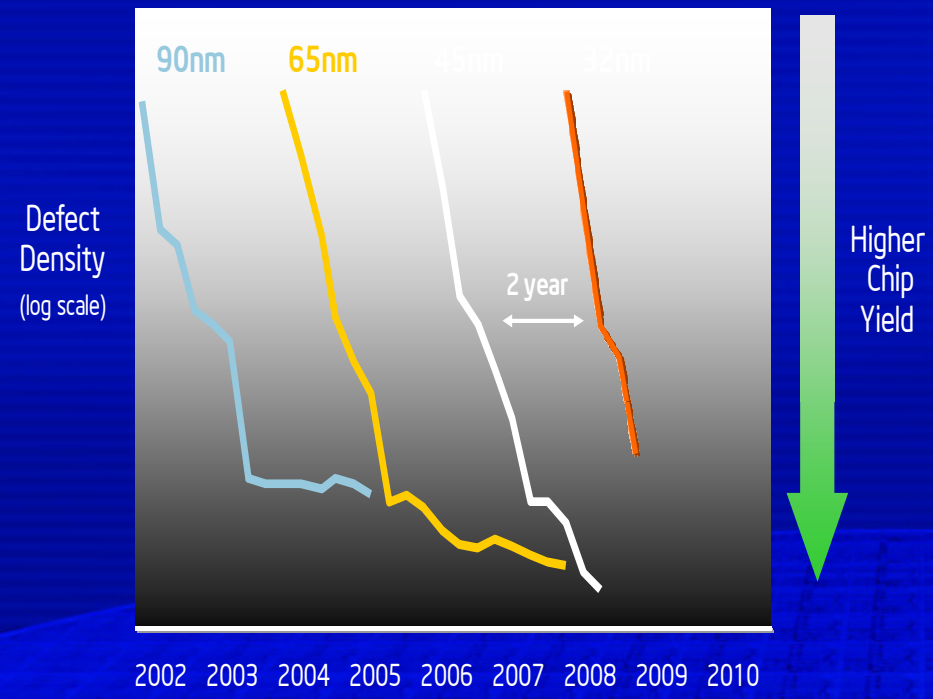


Process trends: New Generation Every 2 Years



Source: Intel

Yield Trends



- 2 year technology cycles
  - High yields
  - Fast ramp to volume
- Progress is not slowing

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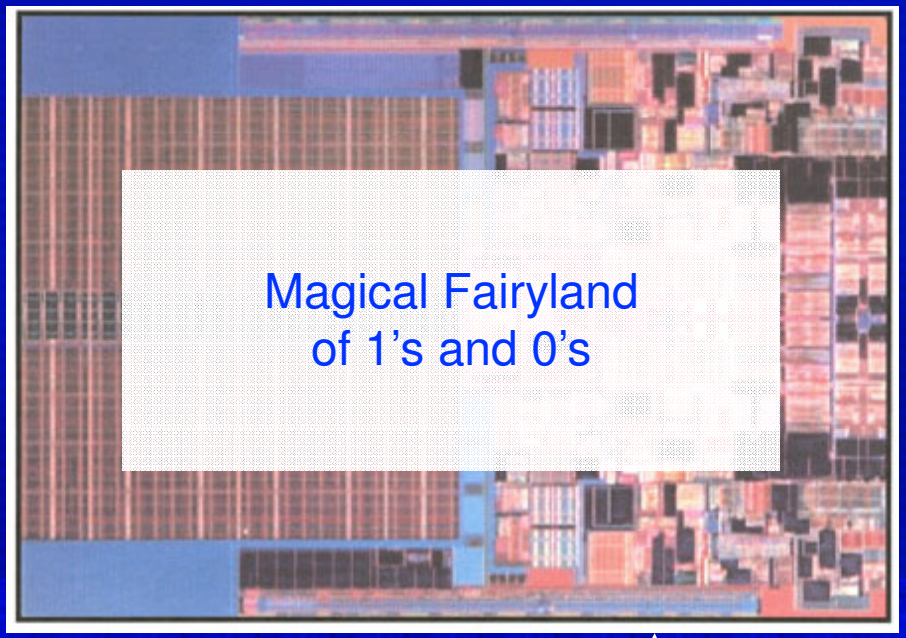
Why Analog Design?

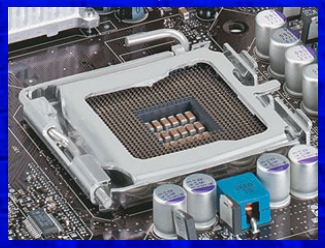
(analog circuits are needed to interface with reality. reality is analog)



Thermal

Configuration

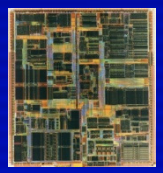
Temporal



Electrical

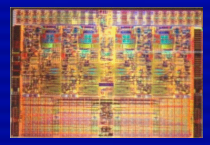
Source:
Rachael Parker

Growth in Analog Circuits



Microprocessor:

clock generator
IO bus
thermal shutdown
trim



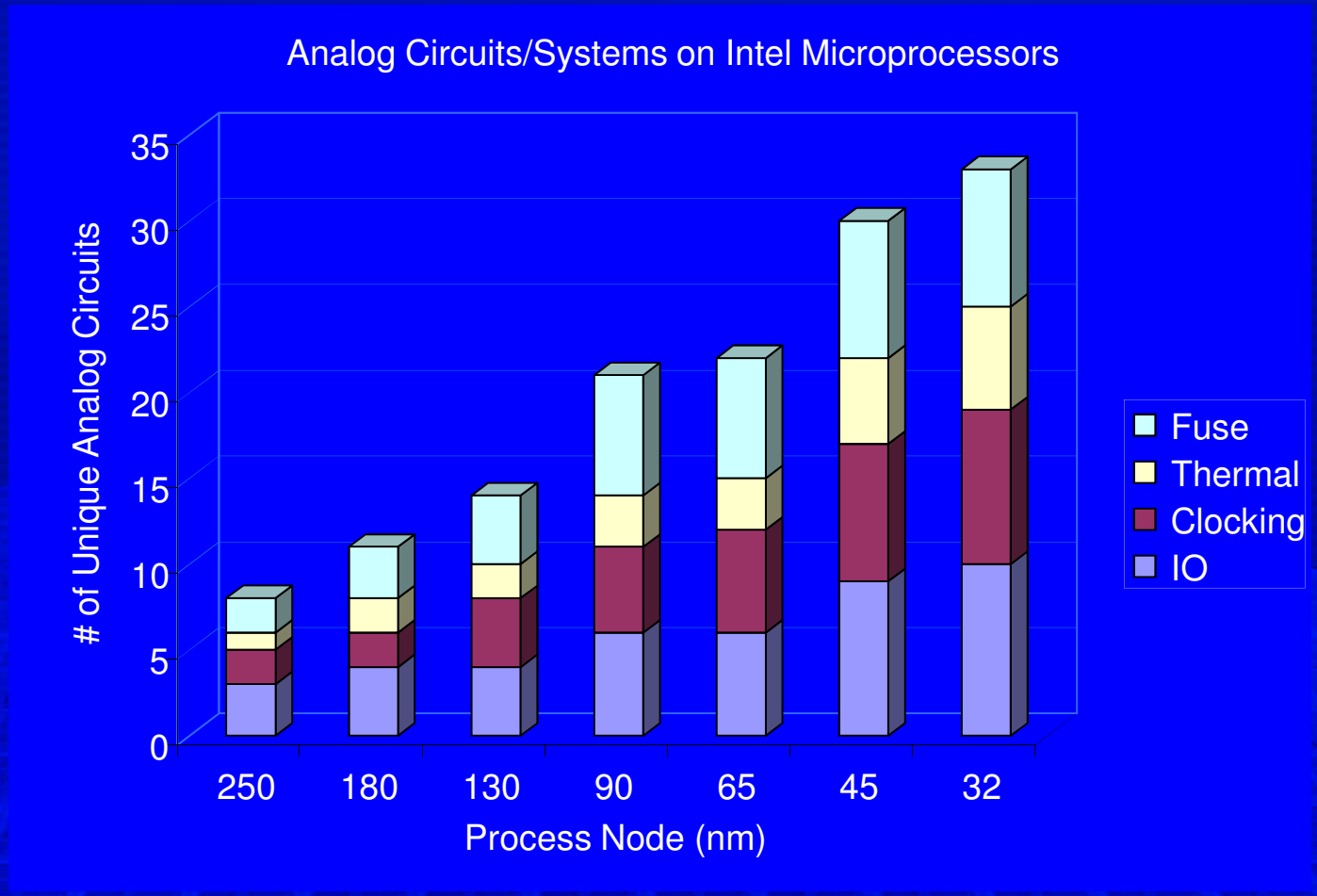
Multi-core SOC:

multi-domain clocking
10-20 PLLs

high speed serial IO
low jitter clock

advanced thermal and
power management

unit-level trim of analog
components



Performance Requirements ~10x over a decade

Pentium® II Processor

- 250 nm
- PLL: 400 MHz Fmax
- DTS: 140 ℃ ± 15 ℃ single trip point
- I/O: 266/400 MT/s

Core™ i7 Processor

- 45 nm
- PLL: 3+ GHz Fmax
- DTS: -10 ℃ to 140 ℃ 1 ℃ Resolution
- I/O: 6400 MT/s

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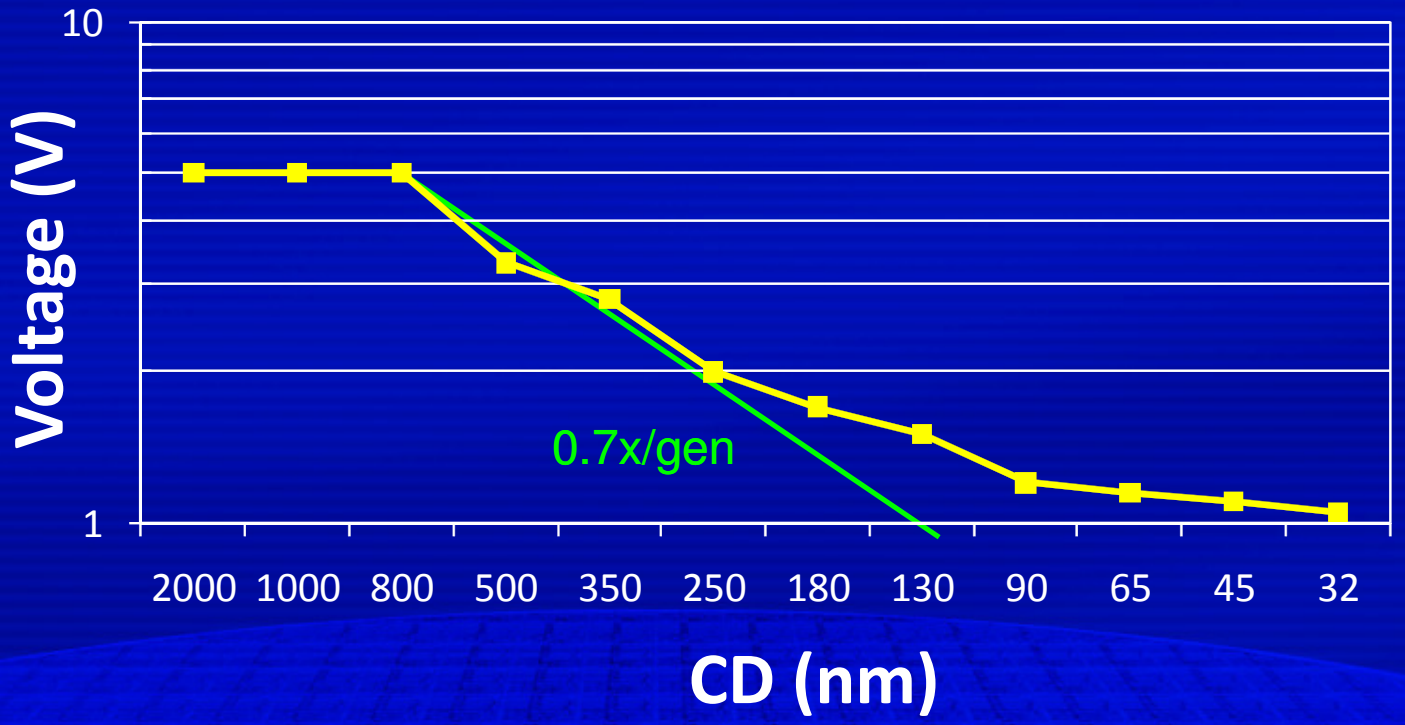
Voltage Scaling



- Voltage scaling has slowed on recent technologies
  - This is the technology maximum voltage

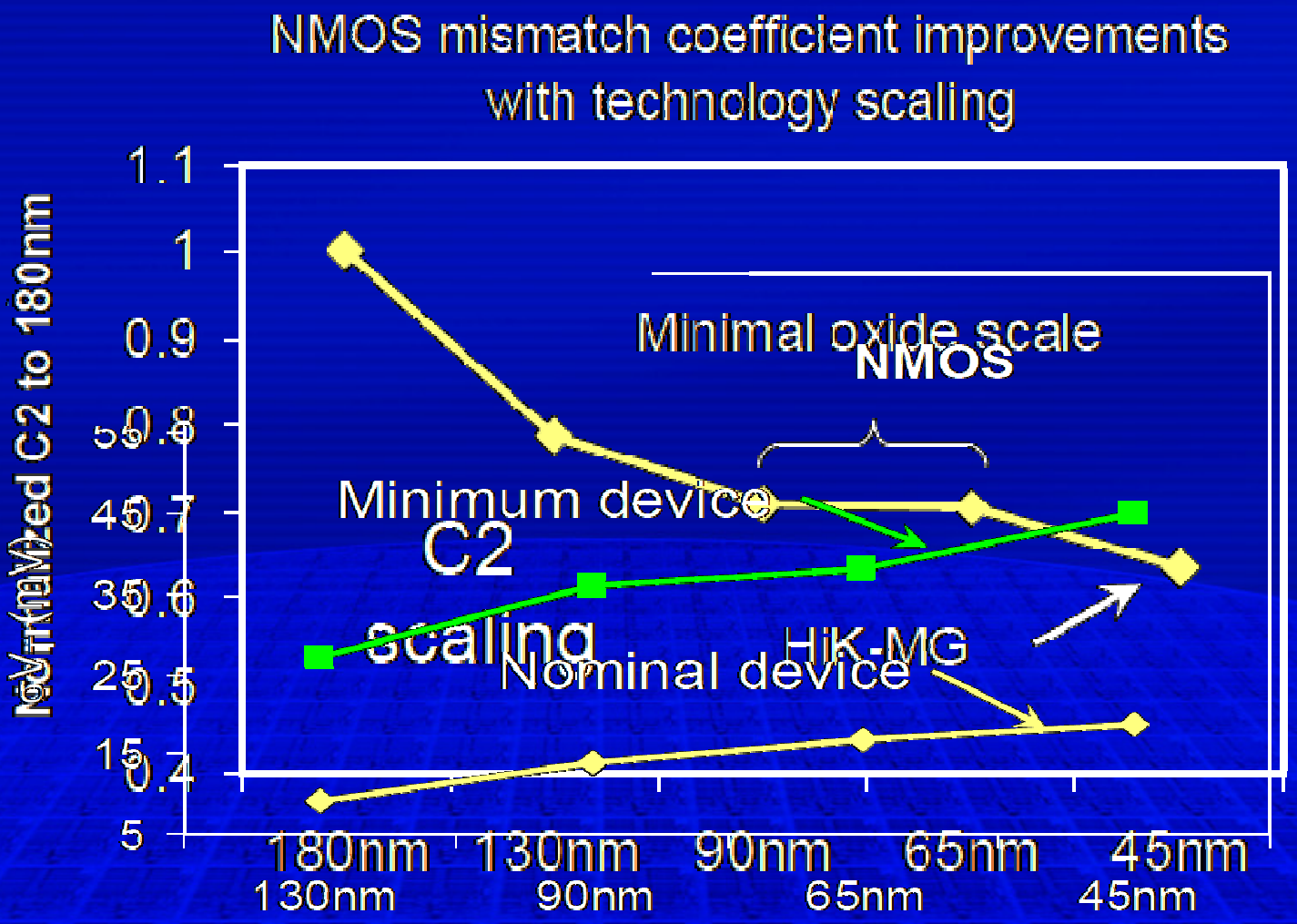
Analog Scaling with Voltage

- Reduced operating range of classical circuits
  - Signal shrinks
  - Noise doesn't
- Low overdrive exacerbates Vt mismatch
- Weakly "off" switches leak

Device Mismatch Trend

- Transistor threshold variation increases with shrinking device size
  - $\sigma V_t = C_2/\sqrt{W_{eff} \cdot L_{eff}}$
- Process improvements provide some relief
  - Scaled device sizes still lead to variation increases

Scaling of σVt Random Variation



– **Kuhn, "Reducing Variation in Advanced Logic Technologies", IEDM 2007**

Noise

- **Thermal noise**

$$\overline{dV_{eq}^2} = 4kT\left(\frac{2/3}{g_m}\right)df \approx \frac{L}{W}$$

- **1/f noise**

$$\overline{dV_{eq}^2} = \frac{KF}{WL \cdot C_{ox}^2}\frac{df}{f}$$

- **Dynamic range decreases for smaller L and W**
  - **Sansen, "Analog IC Design in Nanometer CMOS Technologies", VLSI Design 2009**

Co-Optimization

- Time to market can force design in parallel with process development
  - The good news is that process development is in parallel with design
- Reserve some adaptability to cover when development does not go as expected
- Note:
  - Digital circuits generally have analog success criteria
  - Analog circuits usually have binary success criteria

Other Challenges

- **Mixed Signal Validation:**
  - **When digital and analog circuits are mixed the validation approaches that are effective for either in isolation fail to adequately cover the combination**
    - **Circuit simulation runs times explode**
    - **RTL simulation doesn't model analog behavior**
- **Testability**
  - **Increasingly difficult to characterize the clock**
    - **Low bandwidth, legacy DFT pins**
  - **Difficult to do volume analog test, yet statistical design requires statistical test**

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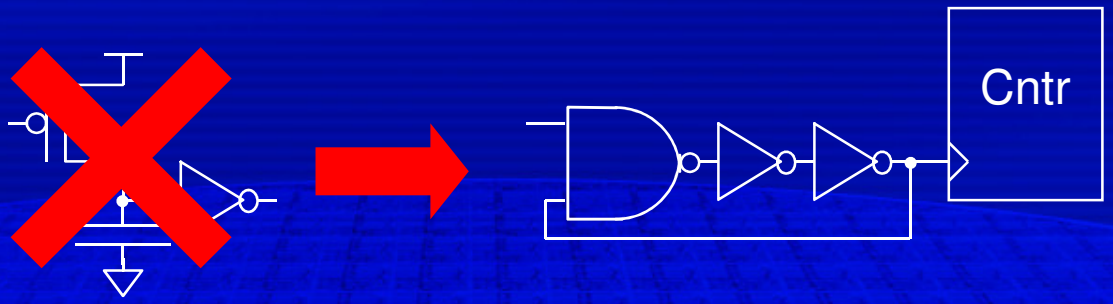
Avoid Analog If You Can

- **Many functions can be implemented with analog or digital approaches**
  - **If possible, choose digital**



Copy* It If You Can't Avoid It

- A new implementation is fun
  - It's also a way to find new kinds of mistakes to make
  - It's more expensive and takes longer than copying
- Take advantage of the work that others have done to find mistakes and validate solutions
  - * Paying attention to IP laws

If You Can't Copy It, Then Apply Good Design Practices

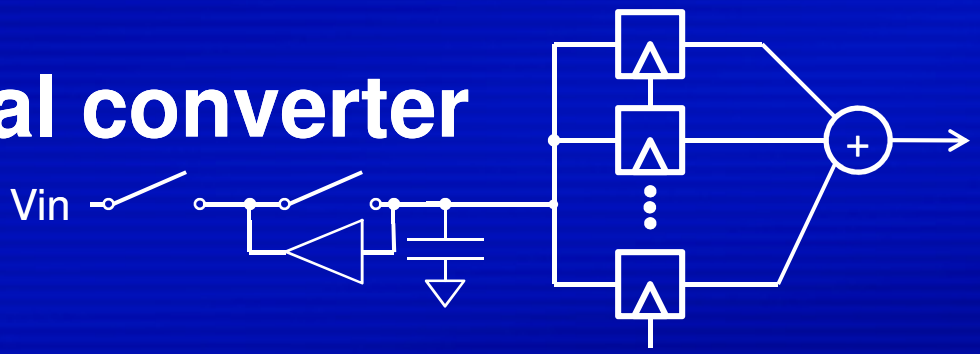
- Keep It Simple!
  - As simple as possible, as digital as possible
- Document your work
  - The flip side of reuse, is that you need to make your own work reusable
  - Documentation improves the quality of design reviews, helping find mistakes sooner
  - People who are reusing your work are invested in finding errors

Good Design Practices

- If you're co-developing along with your process, build in lots of tolerance for process targeting
- Build in tolerance for variation
  - There are only so many atoms available in those transistors
  - Keep matching localized
- Utilize self calibration, trimming, and fuse options
  - This will help increase tolerance to retargeting and variation

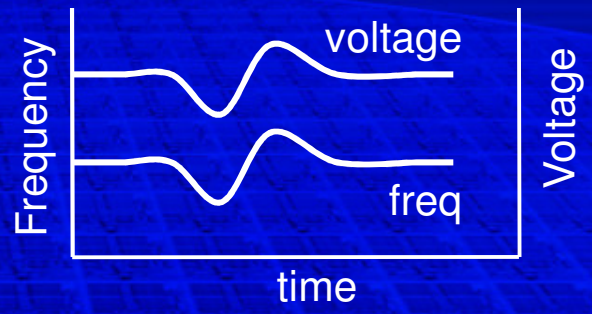
If You Can't Fix It, Feature It

- **Analog to digital converter**



  - **Daly, "A 6b 0.2-to-0.9V Highly Digital Flash ADC with Comparator Redundancy", ISSCC 2008**

- **Adaptive frequency clocking**



  - **Kurd, "Next Generation Intel Micro-architecture (Nehalem) Clocking Architecture", JSSC 2009**

Statistical Design

- Increasing device variation requires variation aware design
  - Worst case design is generally not practical
  - Skew corner simulation does not highlight the impact of within die variation
- Statistical design techniques help predict and understand the impact of variation
  - Monte Carlo
  - Design of Experiments
  - These tools don't replace the need for engineers to understand statistics!

Validation Is Essential

- Circuit simulation
  - It's the time honored approach
    - Necessary, but not sufficient in a mixed signal system
- Mixed signal validation
  - RTL is often discrete time, discrete voltage
  - Hybrid circuits control RTL invisible behavior
    - Impedance, delay, temperature, voltage, current
- Design reviews
  - Reviewer team needs to have variety and engagement

AMS Validation

- Ensure that individual analog blocks work
  - The traditional realm of circuit simulation
- Ensure that analog blocks work together
  - Not just at the center of the spec range
- Ensure that digital and analog work together
  - Both control and data flow

Other Rules of Thumb

- Need to enforce supply isolation between analog and digital circuits
- Production vs. simulation schematics
  - It's tempting to make "alternate" schematics for simulation that include extras
    - Don't
  - If necessary build a test bed in a higher level of hierarchy

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Conclusion

- We are increasing the scope and complexity of analog circuits on logic processes
  - At the same time those processes are becoming harder to work with
  - → Eliminate unnecessary analog design
  - → Avoid making analog the limiter where possible
    - floorplan constraints, timing margin…
  - → Mitigate process scaling non-idealities
    - Trim, offset cancellation, noise shaping, high voltage analog, etc
  - → Don't skimp on mixed signal validation

Questions?