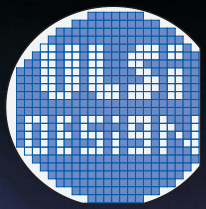
23rd International Conference On VLSI Design

9th International Conference On Embedded Systems



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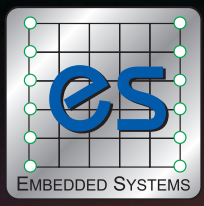

Theme: Affordable Technology For Emerging Markets

January 3 - 7, 2010
NIMHANS Convention Centre
Bangalore, INDIA

Sponsored by
VLSI Society of India (VSI)

Technical Co-sponsors
IEEE Circuits And Systems Society (CASS)
ACM Special Interest Group on Design Automation (SIGDA)

In Co-operation with
IEEE ED/SSC/CAS Societies Bangalore Chapters

VLSID 2010 CONFERENCE

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Message from General Chairs

Welcome to **VLSID 2010**, which marks the 23rd year of International Conference on VLSI Design and the 9th year of International Conference on Embedded Systems. This conference has become an annual highlight in the calendar of the semiconductor ecosystem world-wide, focusing on innovations, best practices and knowledge sharing in chip design, electronic design automation, and embedded system communities.

This year, we bring the conference back to Bengaluru (or Bangalore), the hub of Indian semiconductor and information technology (IT) industries, the city best known as Silicon Valley of India. Having the 2010 conference at Bangalore also commemorates a special occasion for the IT industry at large – In 1985, Texas Instruments became the first multinational to set up base in Bangalore, and the 2010 conference celebrates 25 years of a thriving industry.

A conference's success is measured by the quality of the technical program it puts together. This year, the responsibility for the technical program has been assumed by the distinguished program chairs, Prof. Niraj Jha from Princeton University, USA and Dr. Rubin Parekhji from Texas Instruments, India. Under their leadership, the technical program committee comprising of experts from industry and academia have put together a formidable 3 day technical program with 70 technical papers after a vigorous review and selection process. In conjunction, we have also endeavored to bring the “best in business” to the conference – The technical program features embedded tutorials, panel and lectures, and keynotes from leaders and visionaries in our fields.

This conference is not complete without its signature events and highlights.

- A 2-day tutorial preceding the main conference that provides a technical deep-dive into hot topics for our engineers, students, and managers.
- A 2-day Industry Forum track that will further the interactions between the semiconductor industry and delegates.
- A 1-day Education Forum track (formerly called student track) that throws open the doors of VLSI education not just to students in this domain, but any new entrants from academia and industry.
- The scope of Design and EDA contest has been expanded this year to have a systems focus as well, and promises to provide a platform to showcase exciting designs, systems and tools being built.
- The Fellowship program continues to facilitate participation to several folks who wish to attend the conference, but need some financial support. This year, we have opened this program to engineers who may be in job transition.
- For the first time the conference will be web cast, enabling remote participation.

The value of this conference to our supporters reflects in the strong sponsorship and exhibits presence even in these economically difficult times. We express our sincere thank you to the sponsors and exhibitors. VLSID is the result of the work of many dedicated volunteers. It is important to acknowledge the tireless efforts of the conference committee team members, who have volunteered their time for more than a year on various activities leading to and at this conference. Organizing a

Message from General Chairs

conference of this scale requires a strong conference organization team - S. Ramesh and R. Madhu have held this conference together seamlessly behind the scenes. We also thank the organizational sponsors VLSI Society of India (VSI), technical co-sponsors IEEE Circuits and Systems Society (CASS) and ACM Special Interest Group on Design Automation (SIGDA), and the local chapters of IEEE ED/SSC/CAS for their support.

On behalf of the conference committee, we once again welcome you to the conference, and hope that you will have an experience that is enlightening, thought-provoking, rewarding, and enjoyable. Thank you all for coming.

Warm Regards,

Mahesh Mehendale
General Co-Chair

Srivaths Ravi
General Co-Chair

Message from Program Chairs

We extend our heartiest welcome to the attendees of the 23rd International Conference on VLSI Design and the 9th International Conference on Embedded Systems being held on January 3-7, 2010 at NIMHANS Convention Centre, Bangalore, India. The theme of this joint conference is "Affordable Technology for Emerging Markets". Under this theme, researchers and designers from all over the world will present and discuss recent advances in a broad array of topics, including computing architectures, VLSI design and test from system to layout, embedded systems, and emerging applications. These topics provide the basic foundations and growth avenues for the semiconductor industry. The conference attracts attendees from the industry, academia, research laboratories and government organisations. It will present to them a snapshot of the state-of-the-art through regular paper sessions, special sessions, embedded tutorial and hot topic sessions, theme based invited talks, keynote speeches, industrial exhibits, and full-day tutorials. The conference theme alludes to the rapid progress being made in emerging markets, where technologies that promote affordability are the keys to success.

The regular paper submissions were arranged in seven tracks: Architectures, VLSI CAD, Front-end Design, Test and Verification, Low-power Design, Circuits and Technologies, and Emerging Applications and Technologies. Each track was chaired by two experts. Several experts from around the world were then requested to serve on these tracks as part of the program committee. We received 320 paper submissions from around the globe this year. The challenge was to whittle it down to the 70 that were accepted for presentation. The international program committee rose to this challenge by working extra hard to provide at least two reviews from the committee and requesting several more from other experts. The total number of reviews received was 1241, for an average of 3.9 per paper. The program committee meetings were held at Bangalore and Princeton on the same day. The aim was to provide at least three reviews for each paper. Barring few exceptions, we were able to meet this goal. A large number of papers actually received many more than three reviews. This would not have been possible without the help and tireless work of hundreds of reviewers who volunteered their time to enable the conference to select the best set of papers possible. We owe a debt of gratitude to all these experts for a job well done. The names of the program committee members have been included in this digest to acknowledge their valuable contributions.

We have included nine embedded tutorial/hot topic sessions in the conference. These will provide an in-depth preview into several emerging areas of vital importance to the semiconductor industry. These include chip design in year 2020, three-dimensional ICs, design flows for systems-on-chip, tackling process variations in ICs, SRAM design in the emerging FinFET technology, robust system design, IC design at 22nm, video coding algorithms and architectures, and microfluidics.

Several eminent speakers have accepted our invitation to deliver keynote speeches in plenary sessions and the banquet

Dimitri Antoniadis, Professor, MIT.
Prith Banerjee, Director, HP Labs.
Hermann Eul, Member of Management Board, Infineon.

Message from Program Chairs

Larry J. Hornbeck, Fellow, Texas Instruments.
Ahmad Bahai, Fellow, National Semiconductor.
Walden C. Rhines, CEO, Mentor Graphics.
Gregory F. Taylor, Fellow, Intel.
Yervant Zorian, Chief Scientist, Virage Logic.

We have also organized a theme session on “Affordable Technology for Emerging Markets” where distinguished speakers talk about application drivers for low-cost technology and embedded systems. An executive panel has additionally been organized, where leading managers and technologists debate issues critical to semiconductor and EDA companies.

We offer our deep appreciation to the tutorial chairs, Preeti Ranjan Panda and Anand Raghunathan, for supervising the review process for selecting seven full-day tutorials and two half-day tutorials, spread over first two days of the conference.

We owe our gratitude to the Steering Committee Chair, Vishwani Agrawal, who has been the guiding light of this conference for more than two decades, to the General Co-chairs, Mahesh Mehendale and Srivaths Ravi, for their sage advice throughout the paper selection process, Publication Chair, C. P. Ravikumar, for helping us meet various publication deadlines, and all other members of the conference committee for their dedicated contributions to the conference. We would also like to thank IEEE CAS, SSC and ED societies as well as VSI and ISA for providing technical co-sponsorship.

It is our sincere hope that you will enjoy and benefit from the assembled technical program.

Niraj K. Jha
Program Co-Chair

Rubin A. Parekhji
Program Co-Chair

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TUTORIALS INFORMATION
Sunday, 3 Jan 2010

The 23rd International Conference on VLSI Design brings to you 7 full-day tutorials and 2 half-day tutorials on a wide range of topics related to VLSI Design, EDA, and Embedded Systems. Recognised experts from both industry and academia around the world will cover the state-of-the-art in various domains. VLSI Conference tutorials are targeted to benefit audiences with diverse backgrounds including students, teachers, and industry practitioners. The 2010 tutorial program also introduces a NEW hands-on tutorial format where participants will be engaged in a more interactive setting.

Tutorial Venues: *Tutorials **T1-T7** will be held in the main conference venue (NIMHANS Convention Center), while hands-on tutorial **T8** will be held at Brahmaputra Training room (3rd Floor), Synopsys (I) Pvt. Ltd., RMZ Infinity, Old Madras Road, Bangalore-16.*

09.00 - 17.00 hrs
AUDI 1

TUTORIAL 1: Green at the Micro Scale: Design and Management of Energy Harvesting Wireless Embedded Systems

PRESENTER: **Vijay Raghunathan -** Purdue University

Description : The field of green computing, which has gained tremendous importance and popularity over the past few years, has mainly focused on large computing systems such as server farms. This tutorial provides an introduction to how the principles of green computing can be applied at the micro-scale, targeting the billions of embedded devices found around us. A promising start in this direction is to power embedded systems using environmental (renewable) energy sources such as solar, wind, vibration, etc., which raises the possibility of self-sustaining embedded systems that can operate perpetually without the need for battery replacement. Such a capability is particularly attractive for embedded systems such as wireless sensor networks that need to operate autonomously for long periods of time (several months to years).

However, designing a highly efficient system to realize the potential benefits of energy harvesting requires an in-depth understanding of several design considerations and tradeoffs. This tutorial will provide an introduction to the area of micro-scale energy harvesting, highlight the challenges involved in architecting self-sustaining embedded systems, and describe various hardware and software techniques for their efficient design and runtime management. As a case study, the tutorial will also describe how these techniques were applied to design the Heliomote solar energy harvesting wireless sensor node.

TUTORIALS INFORMATION
Sunday, 3 Jan 2010

09.00 - 17.00 hrs
AUDI 2

TUTORIAL 2: New Generation Integrated Multi-Core Modeling in Microprocessor Design

PRESENTERS: **Pradip Bose, Vaidyanathan Srinivasan, Viji Srinivasan, Sriram Vajapeyam -** IBM

Description : Pre-silicon performance modeling in the 21st century has quickly evolved, out of technology-driven necessity, into an integrated modeling art or science. No longer is it meaningful for architects to study performance (IPC) sensitivities in isolation, while product quality metrics like power, temperature and reliability are modeled only in late-stage design. With cycle-accurate performance models augmented with the burden of also projecting the above other quality-related metrics, issues related to simulation speed and analysis accuracy get magnified by a large factor. In this tutorial, we propose to present the modern challenge of integrated pre-silicon modeling and validation from the perspective of real industrial microprocessor design projects. We will also examine the techniques to model the benefits (and performance degradations) derived from on-chip power, temperature and reliability management devices within the framework of current generation multi-core integrated models. We will discuss methods of validating pre-silicon integrated models and present real data to illustrate the errors that can result from inadequate high-level abstractions during early-stage modeling. We will cover academic research concepts that have benefited or influenced industrial practice in all aspects of the above problem, and we will point to open research issues and problems that need to be solved – especially in the context of technological changes brought forth by 3D chip integration.

09.00 - 17.00 hrs
AUDI 3

TUTORIAL 3: Design- process optimization challenges at the Bleeding Edge (or Why can't I design what I want in 22nm technology?)

PRESENTERS: **James Oberschmidt, Josef Watts, Suresh Purayat -** IBM, **J. Andres Torres -** Mentor Graphics

Description : As VLSI technology scales from 65 nm to 45nm to 32nm and beyond, both timing and power performance of integrated circuits are increasingly affected by process variations. Systematic components of the variations are generally traceable according to process models while random variations are traced in process corner-based methodologies.

This tutorial will cover the factors in sub-resolution lithography affecting this paradigm shift which demands a strong need for design technology to interact in early stages and devise co-optimization techniques. It will also cover important methodologies such as incorporation of tools into the design flow that will enable reduction of PV (process variation) bands and cut down the learning cycles at process development stage by early

interception of this process knowledge at the design phase. Introduction will be made to predictive modeling techniques and physical design alteration through reverse engineering at mask level to print the desired shapes on the wafer. Demonstrations and real life examples of need for OPC (optical proximity corrections), and ORC (optical rule checks) will also be provided. Preliminary results of challenges introduced by layout induced stress compensation are also incorporated for discussion about their relevance to sub 32nm process technologies.

09.00 - 17.00 hrs
BOARD ROOM

TUTORIAL 4: High-Quality and Low-Cost Delay Testing for Nanoscale CMOS Technologies

PRESENTERS: **Krishnendu Chakrabarty -** Duke University,
Mohammad Tehranipoor - University of Connecticut

Description : As technology scales to 32nm and clock frequency and chip density continue to rise, new challenges are emerging in the area of VLSI testing and design-for-testability. Test engineers must now deal with a number of difficult problems such as the effects of IR-drop and power supply noise (PSN) on chip performance, signal integrity and crosstalk effects on path delay, high test-pattern volume, low fault/defect coverage, test generation and fault simulation for small-delay defects, process variation effects, high test cost, and unmodeled defects. This full-day tutorial will provide practice-oriented solutions to the above challenges. The tutorial is designed to provide design and test engineers with in-depth knowledge on high-quality delay testing methods for reducing defect escapes and increasing in-field reliability.

TUTORIALS INFORMATION
Monday, 4 Jan 2010

09.00 - 17.00 hrs
BOARD ROOM

TUTORIAL 5: Thermal Modeling and Management for 2D and 3D Multiprocessor System-on-Chip

PRESENTERS: **David Atienza -** EPFL, **Ayse Coskun -** Boston University, **Jose Ayala -** Complutense University of Madrid

Description : Multi-Processor Systems-on-Chip (MPSoCs) are penetrating the consumer electronics market as a powerful solution to answer the strong and steadily growing demand for scalable and high performance systems, at limited design complexity. Nevertheless, MPSoCs are prone to alarming temperature variations on the die, which seriously decrease their expected reliability and lifetime. Furthermore, technical advances in manufacturing technologies are fueling the trend towards more powerful 3D MPSoC designs. However, 3D stacking creates higher power and heat density, leading to degraded performance if thermal management is not handled properly. Thus, it is critical to develop dedicated new design methodologies that can guarantee a thermally controlled behavior of forthcoming 2D and 3D MPSoCs.

This tutorial, which is divided in four parts, covers the development of dedicated design methodologies for MPSoCs that seamlessly address their thermal modeling, analysis and management. In the first part, we revise different thermal behavior exploration and modeling mechanisms for MPSoCs based on simulation and emulation frameworks. Then, in the second part, we introduce the concept of thermal-aware micro-architecture and latest compilation techniques for thermal balancing of MPSoCs. Next, in the third part, we discuss reactive and proactive run-time thermal management methods, which achieve thermal runaway prevention while incurring negligible performance degradation. Finally, in the fourth part, we cover new active thermal modeling and active management methods (liquid cooling-based) for 3D MPSoC architectures, developed in cooperation with IBM.

The main concepts of the different parts of the tutorial are illustrated by industrial case studies based on Sun's UltraSPARC T1, Freescale Multimedia-SoCs and IBM 3D-stacked chip prototypes.

09.00 - 17.00 hrs
AUDI 2

TUTORIAL 6: Model Based Design, Verification and Testing for Embedded Control Systems

PRESENTERS: **Ambar Gadkari, Ramesh S -** General Motors India Pvt. Ltd,

Description : Embedded control systems have become all pervasive ranging from domestic appliances to highly safety-critical control applications in avionics & automotive domains and industrial automation,

robotics and so on. In the competitive market scenario it is evident that the development of such systems should be highly reliable leading to "first-pass successes" irrespective of safety-criticality of the end product. Model based development adopted for embedded control systems provides the means for systematic design and validation of the complex systems using automated flows. Model based design helps not only in uncovering the design and requirement issues at early stages but also enables automatic generation of the software code and test cases for guaranteeing high quality implementations. Additionally, having well structured approach for requirements and design modeling can help in introducing formal verification techniques to ensure high confidence and reliability of these artifacts.

In this tutorial we plan to introduce the audience to various methods and techniques developed for embedded control software for modeling the requirements and design, formal verification, simulation based validation and model based testing of the implementation. We intend to illustrate the modeling formalisms and methods through real-life examples. A brief overview of the commercial and research tools used in automotive embedded control software development would be provided along with few a pointers to the present challenges and the

09.00 - 12.30 hrs
AUDI 3

TUTORIAL 7A: Wired interfaces design *(half day)*

PRESENTERS: **Sakthi Prashanth, Mayank Goel, Ravula Lakshmi -** Infineon Technologies Pvt Ltd

Description : Interface (IO) design is a sub-domain of analog circuit design which is increasingly becoming complex and thereby challenging and exciting. One frequently comes across terms like USB, HDMI, DDR which are a few of the popular interface standards. This tutorial provides an insight into what these are, why we need them and what goes into these designs. The tutorial starts by answering a simple question, "What is an IO?" and goes on to provide an in depth look at the building blocks of an IO, different types of IOs and their applications.

The tutorial further explores challenges commonly faced by an IO designer such as transmission line effects, supply & ground noise, over-voltage tolerance, hot swapping, ESD & latch up, EMI, etc. Commonly used circuit design techniques to overcome these challenges are introduced. These include techniques like slew rate control, impedance matching and calibration, failsafe circuits, ESD clamp circuits, etc. The tutorial ends by providing a peek into advanced topics of high speed serial interfaces and gigabit PHYs.

TUTORIALS INFORMATION
Monday, 4 Jan 2010

13.30 - 17.00 hrs
AUDI 3

TUTORIAL 7B: High PPAY Embedded Memories Design & Test *(half day)*

PRESENTERS: **Murugeswaran Surulivel, Sudhir Moharir -** ARM

Description : The world has been designing memories for a long time. It has become more and more difficult to design embedded memories that work reliably inside big chips like microprocessors at advanced process nodes. The percentage of memories in SOC chips has been constantly increasing. With the technology nodes making leaps from 180nm to 22nm, designing memories that deliver high yield is not a trivial task. With bitcell leakages increasing, delivering the performance that is required for today's applications is difficult. Keeping up with the low power expectations of the mobile world is challenging. Satisfying customers with diverse requirements of high performance, low power, high density and good yield is extremely challenging. It is most important that we not only design the memories well and implement them correctly in the layouts, these memories also need to be tested and silicon qualified before delivering to the customers so that their designs become successful at the first time.

This tutorial presents different aspects of achieving high PPAY embedded memories. High PPAY denotes high Performance, low Power, low Area, and high Yield. The tutorial will cover different architectures targeted at high speed, high density, and low power. Whatever the architecture, high yield is a common requirement. The basics of margin methodology and the variability analysis will be discussed so as to guarantee high yield and robust functionality. The Design For Manufacturability (DFM) guidelines will be discussed to achieve better yield from layouts. How we test the memories and how we do a Failure Analysis, as and when needed, will be discussed. This tutorial also covers memory test and repair structures, memory Defect Based Testing (DBT), and MBIST/R (Memory Built In Self Test and Repair) architecture for improving the yield. Optimized memory test patterns and efficient repair algorithms are discussed for various types of memories using redundancy.

09.00 - 17.00 hrs
SYNOPSYS

TUTORIAL 8: Low Power design Verification using IEEE P1801 aka UPF *(hands-on tutorial)*

PRESENTERS: **Srikanth Jadcherla, C. V. Sesha Sai Kumar, Neha Bajaj -** Synopsys

Description : As the designs move towards lower geometries, leakage currents dominate leading to increased power consumption at functional and standby modes. Keeping the statutory regulatory bodies, like energy STAR recommendations in mind, the lowest stand-by-power and reduced dynamic consumption is the target for all designs. Voltage is the

key control, along with the switching activity, to achieve low power consumptions. Though the designs have been churned out with in-house methodologies using multi-voltage techniques, they are not scalable when complexity of power management grows or number power and voltage domains increase.

Designing chips that are ultra low power increases the design complexity with introduction of power management units, protection devices etc, that can cause nontraditional low power bugs. Low power design verification gets more complex, when multiple voltage/power states exist and designs can make valid/invalid transitions among these states. Verification need to take care of design functionality not just in power states but transitions as well. Bugs can creep in while changing from one power saving mode to another power saving mode or full functional mode.

This tutorial aims at introducing low power design concepts and bugs that can creep in. One of the important steps in LP designs is capturing the power intent in a format that is reusable, scalable. We introduce IEEE P1801 aka UPF to capture the design power management information. LP verification through dynamic simulation and voltage rule checking is introduced using MVSIM and MVRC respectively.

KEYNOTES INFORMATION
Tuesday, 5 Jan 2010

09.30 - 10.15 hrs

KEYNOTE 1: Nanoelectronics challenges for the 21st century

PRESENTER: **Professor Dimitri Antoniadis -** MIT

Description : Leading edge CMOS technologies today are unique examples of nanoscale engineering at an industrial scale. As we celebrate this remarkable achievement of our industry that forms the ever-expanding technology basis of modern society we cannot help but ponder the question of how we can continue to push the envelope of nano-electronics. With the end of Si FET scaling appearing increasingly near, searching for more scalable transistor structures in Si and in "beyond-Si" solutions has become imperative; from relatively "easy" transitions to non-planar Si structures, to the incorporation of high mobility semiconductors, like Ge and III-V's, to even higher mobility new materials such as carbon nanotubes, graphene, or other molecular structures. And even further, there are searches for new information representation and processing concepts beyond charge in FETs, as for example, in spin-state devices. Of course, declaring silicon dead is premature at best, and with this in mind I will discuss the challenges and possible scenaria for the introduction of novel nano-electronic devices.

10.15 - 11.00 hrs

KEYNOTE 2: Deep Submicron CMOS Technology – the challenges for semiconductor IDM

PRESENTER: **Dr. Hermann Eul -** Member of Management Board, Infineon

Description : Mobile Internet is becoming one of the key future revenue engines. It will be driven by a strong demand of business users, as well as users in emerging countries who do not have computers and want to access internet by hooking up with their cell phones. This trend comes along with continuous cost pressure and ongoing feature integration calling for deep submicron CMOS technology. In a first step, the presentation will give a short summary of the paradigm shifts in the "mobile world" from voice calls to data transmission and the current situation in the renascent mobile ecosystem. The entry of powerful internet and consumer brands and now even luxury designer brands into the mobile handset arena marks the start of a new era which changes the dynamics in this field and results in a stronger battle than ever to control the wireless value chain. The changes of the value chain has strong impact on semiconductor IDMs. It is necessary for the IDM to re-think the value proposition on manufacturing, the entire R&D value chain, and the application support. Differentiation must be achieved on process technologies which are shared with partners or even competitors. The presentation will show how the IDM can respond to these challenges. It will elaborate on new fab strategies and and new models for the R&D set up. It will give examples for successful product differentiation on standard CMOS technologies such as massive System-on-Chip integration requesting a high level of circuit innovation.

KEYNOTES INFORMATION
Tuesday & Wednesday, 5 & 6 Jan 2010

13.45 - 14.30 hrs

KEYNOTE 3: DLP® technology: Extreme Versatility

PRESENTER: **Dr. Larry J. Hornbeck -** Fellow, Texas Instruments

Description : Microelectromechanical systems (MEMS) technologies are bringing value to many industrial and consumer products in the way of improved functionality and miniaturization. An example is the Digital Micromirror Device, a high-density array of up to two-million micromirrors with associated CMOS memory cells integrated together on a silicon chip. The synergistic combination of the DMD chip with optics and algorithms gives DLP® projection display technology a unique nature – the versatility to be leveraged over a broad range of applications. Today DLP technology enables the tiniest products (embedded in mobile phones), the brightest products (over 30,000 lumens) and virtually everything in between – all with leading world-class image quality. The keynote address will provide an overview of the origins and workings of the technology and an understanding of traditional and new market applications.

08.30 - 09.15 hrs

KEYNOTE 4: Delivering 10X Design Improvements

PRESENTER: **Dr. Walden C. Rhines -** CEO, Mentor Graphics

Description : Time and time again, escalating complexity has threatened to derail the IC industry from the extraordinary 35% annual reduction in transistor pricing it has enjoyed the past 40+ years. Fortunately, in each and every instance, creative engineers and companies have seen this as a challenge and opportunity to innovate. As a result, the electronic design automation industry has repeatedly delivered order of magnitude improvements in every aspect of the IC design cycle for over three decades.

Today, the exponential rise in complexity has quickened its pace as the industry moves toward adoption of 28 nm and below. Dr. Wally Rhines will discuss how in the next five years, 10X improvements in design methodologies are needed in four principal areas: high-level system design, verification, embedded software development, and back-end physical design and test. He will provide a roadmap for the next wave of changes needed to successfully negotiate rising complexity, highlighting where they will most likely occur.

All keynotes in AUDI 1

KEYNOTES INFORMATION
Wednesday, 6 Jan 2010

13.40 - 14.25 hrs

KEYNOTE 5: Future Research Directions in Electronic Design Automation

PRESENTER: **Dr. Prith Banerjee -** Director, HP Labs

Description : Electronic Design Automation (EDA) is the category of tools for designing and producing electronic systems ranging from printed circuit boards (PCBs) to integrated circuits. Today, electronic design automation develops automated tools for designing integrated circuits but there is a need to address automation for electronic systems at higher levels. This talk will discuss some promising areas for future research in the area of electronic design automation. The proliferation of new modes of communication and collaboration has resulted in an explosion of digital information. To turn this challenge into an opportunity, the IT industry will have to develop novel ways to acquire, store, process, and deliver information to customers — wherever, however, and whenever they need it. An intelligent IT infrastructure — which can deliver extremely high performance, adaptability and security — will be the backbone of these developments. At HP Labs, we are taking a multidisciplinary approach to this problem by spanning four areas: computing, storage, networking and nanotechnology. We are working on the design of an Exascale data center that will provide 1000X performance while enhancing availability, manageability and reliability and reducing the power and cooling costs. We are working on the design of a Sustainable Data Center that reduces Total Cost of Operation (TCO) and carbon footprint while meeting current quality of service goals; this requires the development of design automation techniques for simultaneously solving the computing, power and cooling requirements in a data center. We are building a cloud-scale, intelligent storage system that is massively scalable, resilient to failures, self-managed and enterprise-grade. We are designing an open, programmable wired and wireless network platform that will make the introduction of new features quick, easy and cost-effective. Finally, we are making fundamental breakthroughs in nanotechnology — memristors, photonic interconnects, and sensors — that will revolutionize the way data is collected, stored and transmitted. To support the design of such an intelligent IT infrastructure, we will have to develop sophisticated system-level design automation tools that will tradeoff system-level performance, power, cost and efficiency.

18.45 - 19.30 hrs (BANQUET)

KEYNOTE 6: Green Energy - Emerging Technologies and their impact in better energy efficiency realization

PRESENTER: **Dr Ahmad Bahai -** CTO, Fellow and Director of Research Labs at National Semiconductor

Description : Information Technology dominated the headlines and innovation forums in 90s. In contrast, Energy and Green initiatives have been highlighted frequently in this decade. The convergence of IT and ET has brought about extremely promising and exciting opportunities for innovation and betterment of our world.

In this talk, Dr. Bahai will point out the significance of this convergence and its implications on technology and research collaboration

KEYNOTES INFORMATION
Thursday, 7 Jan 2010

09.00 - 09.45 hrs

KEYNOTE 7: Future of Analog Design and Upcoming Challenges in Nanometer CMOS

PRESENTER: **Dr. Gregory F. Taylor -** Fellow, Intel

Description : This work will look at scaling trends in analog circuits, logic processes, and where those trends may be leading us. As microprocessors and Systems on a Chip increase the portions of systems that are being integrated, the number and variety of analog circuits that are needed on a single chip are growing. At the same time, for reasons of cost, performance, and power the manufacturing of these die is being scaled to ever smaller feature sizes. What are the implications of the intersection of these scaling trends and how can we deal with those implications?

13.45 - 14.30 hrs

KEYNOTE 8: Managing IP for SOCs at Advanced Process Nodes

PRESENTER: **Dr. Yervant Zorian -** Vice President & Chief Scientist, Virage Logic

Description : As we navigate through the nanometer landscape, the SOC manufacturability challenges are tremendous. The impact of advanced process nodes on yield, reliability and time to volume is forcing managers to select IP solutions that eliminate the risks and helps ensure optimum yield, superior quality and greater reliability. This presentation discusses today's SOC challenges and introduces strategies to manage IP risk, as we navigate through the new process nodes.

EMBEDDED TUTORIALS INFORMATION
Tuesday, 5 Jan 2010

16.10 - 16.55 hrs
BOARD ROOM

Track A / Embedded Tutorial 1: Electrical modeling of imperfect lithographic patterning

AUTHORS: **T. B. Chen, R. Ghaida, P. Gupta -** University of California, Los Angeles

Description : Due to aggressive scaling of device feature size to improve circuit performance in the sub-wavelength lithography regime, wire, diffusion as well as poly gate shapes can deviate from perfect rectangles. A wafer-shape based power and performance signoff is desirable for RET validation as well as for “closest to- silicon” analysis. Existing compact device models (or interconnect extraction methods) do not handle complicated non-rectangular geometries. Thus, analyses of power/performance for non-rectangular silicon contours are required.

Example aspects include:
- Polysilicon gate imperfections which cause local gate-length changes (e.g., LER).
- Diffusion shape imperfections (e.g., resulting from power/ground rail connections).
- Line-end patterning flaws that manifest as, e.g., catastrophic line-end shortening or rounded lineends.

The standard approach to modeling a non-rectangular transistor is to approximate it by an equivalent rectangular transistor. This permits straightforward use of existing SPICE-based (modeling, simulation) infrastructure. Such models can find variety of uses at various levels in the design to manufacturing flow. The use models can range from electrically driven OPC methods and design rule optimization to cell library characterization and full-chip timing/power analyses. Such models can be, interestingly, used to optimize shapes of transistors or interconnect as well (rectangular shapes don’t have the best power-delay tradeoff!). Chip-level use of such models poses several problems (e.g., simulation runtime, instance uniquification, etc).

This tutorial will discuss comprehensive electrical modeling of non-rectangular devices as well as their use in design/manufacturing flows. Future lithographic patterning is going to add more sources of variation. For instance, double patterning, a 32nm lithography candidate can lead to increased linewidth or spacewidth variability coming from overlay errors; and lead to bimodal variability distributions. Finally, we will briefly introduce other emerging sources of layout-dependent variability such as

EMBEDDED TUTORIALS INFORMATION
Tuesday, 5 Jan 2010

16.10 - 16.55 hrs
AUDI 1

Track B / Embedded Tutorial 2:Robust system design

AUTHOR: **S. Mitra -** Stanford University

Description : Robust system design ensures that future systems continue to meet user expectations despite rising levels of underlying disturbances.

This paper discusses two essential aspects of robust system design:
1. Effective post-silicon validation despite staggering complexity of future systems.
2. Cost-effective design of systems thatovercome CMOS reliability challenges through built-in tolerance to errors in hardware during system operation.

16.10 - 16.55 hrs
AUDI 2

Track C / Embedded Tutorial 3: Chip of 2020: Designing low-cost energy-efficient complex systems using heterogeneous components

AUTHORS: **K. Roy, B.Jung, A.Raghunathan -** Purdue University

Description : Moore's law has provided a metronome for semiconductor technology over the past four decades. However, when CMOS transistor feature size and interconnect dimensions approach their fundamental limits, aggressive scaling will no longer play a significant role in performance improvement. How should the semiconductor industry provide new value in each generation of products in such a scenario? While Moore's law driven scaling has traditionally focused on improving computation performance (through faster clock frequencies and recently, more parallelism), the need for the electronic systems of the future is multi-functional. We envision that integrated systems of the future will perform diverse functions (in addition to high-performance computation and high-bandwidth communication) such as high-accuracy sensing of real-time signals, energy harvesting, and on-chip chemical/biological testing, to name a few. Enabling such diverse functionality with high performance, high reliability and a low energy budget in a single system requires a radical shift in the principles of system design and integration. Instead of focusing on improving the performance of traditional digital CMOS circuits (More than Moore) or exploring nanotechnologies for Silicon and CMOS replacements (Beyond CMOS), we espouse cohesive design and integration of multiple device technologies and diverse components in a single heterogeneous system that is high-performance, energy-efficient and reliable. We will outline our vision in this direction, and support it with illustrative design scenarios where heterogeneous components are used to monitor the health of an electronic system, enable more effective power management, and communicate wirelessly on-chip.

EMBEDDED TUTORIALS INFORMATION
Wednesday, 6 Jan 2010

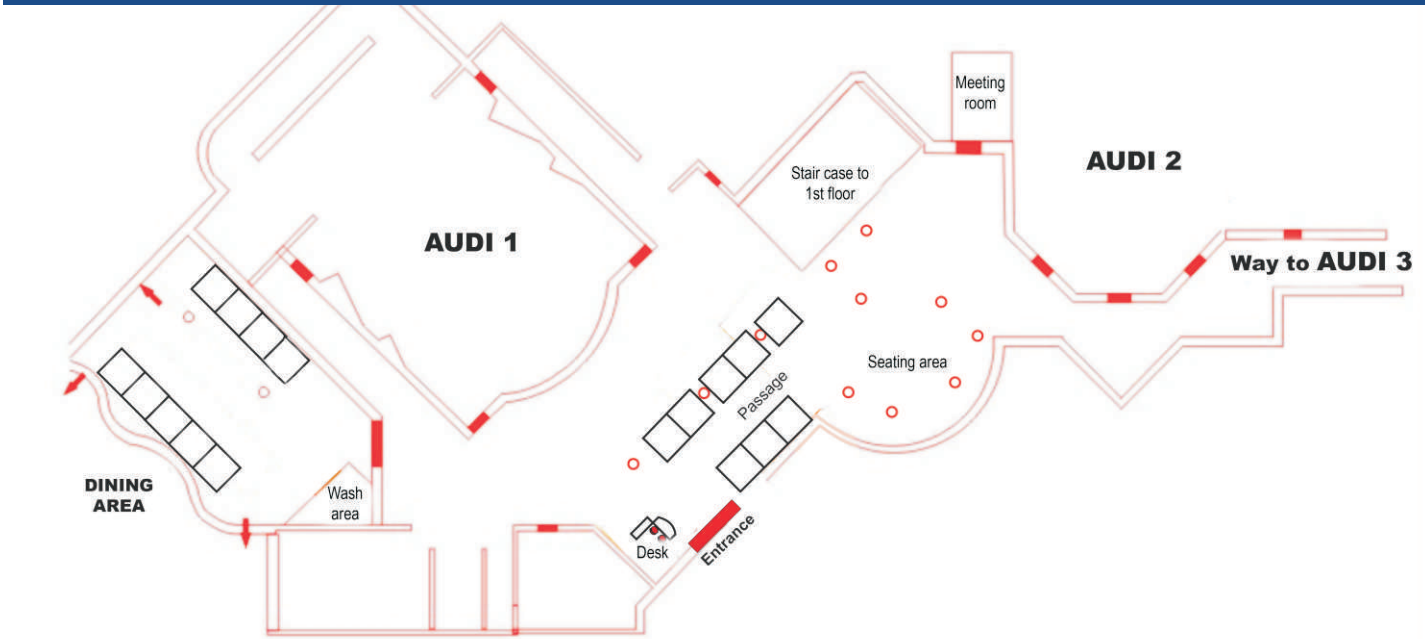
14.30 - 15.15 hrs
AUDI 1

Track A / Embedded Tutorial 4: New world order at the dawn of 22nm era

AUTHOR: **R. Puri -** IBM

Description : Technology scaling clearly has been the driver of semiconductor and thereby EDA industry. In the semiconductor industry today, 45nm CMOS designs are in full production and 32nm design rules and infrastructure is already in place for designs starting later this year. It will not be long before the beat of 22nm will be upon us. Due to ever increasing cost of doing design, design productivity and more specifically, cost of design has become a major bottleneck in large scale design projects. Due to this cost crunch, automated synthesis techniques have been gaining ground on manual and cost intensive (although potentially yielding higher quality of results) custom techniques. The push towards system level performance with multiple lower performance cores as opposed to single high performance core is also making the pursuit of frequency at any cost meaningless. Synthesis vs Custom has traditionally been a lively debate in microprocessor companies but now it is becoming more widespread with the desire of fabless companies to more fully utilize the technology node in order to compete with integrated design and manufacturing houses by utilizing more custom techniques. In addition, now that the physical limits are beginning to impact scaling, the question is: how can we design cost effectively design with complicated technology requirements presented by 22nm node and how the design automation community can help to achieve this goal? What are the challenges at 22nm and what would design look like going into 22nm and beyond? In this talk, we will focus on the design and CAD challenges associated with 22nm and beyond.

VENUE LAYOUT - GROUND FLOOR



23rd International --> VLSID 2010 Conference

Sunday, 3 Jan 2010

09.00 - 05.00 hrs	**Session T1:** Green at the Micro Scale	**Session T2:** New Generation Integrated	**Session T3:** Design-process optimization	**Session T4:** High-Quality and Low-Cost Delay

Monday, 4 Jan 2010

09.00 - 05.00 hrs	**Session T5:** Thermal Modeling and Management	**Session T6:** Model Based Design	**Session T7A:** Wired interfaces design	**Session T7B:** High PPAY Embedded Memories Design	**Session T8:** Low Power design

Tuesday, 5 Jan 2010

07.30 - 08.45 hrs	REGISTRATION			INDUSTRY FORUM
08.45 - 11.00 hrs	PLENARY SESSION			
09.30 - 10.15 hrs	**TECHNICAL KEYNOTE 1** - DIMITRI ANTONIADIS (MIT)			
10.15 - 11.00 hrs	**TECHNICAL KEYNOTE 2** - HERMANN EUL (Infineon)			
11.30 - 12.45 hrs	**Session A1:** Clocking and Physical Design	**Session B1**: Application-specific Architectures	**Session C1:** High-speed Links	
13.45 - 14.30 hrs	**TECHNICAL KEYNOTE 3** - LARRY HORNBECK (Texas Instruments)			
14.35 - 15.50 hrs	**Session A2:** Analog / RF CAD	**Session B2:** Efficient System Modeling and Design	**Session C2:** Circuit Design and Modeling I	
16.10 - 16.55 hrs	**Session A3:** Tackling Process Variations	**Session B3:** Robust Design	**Session C3:** Chip 2020	
17.00 - 18.00 hrs	EXECUTIVE/CTO PANEL			

Wednesday, 6 Jan 2010

08.30 - 09.15 hrs	**TECHNICAL KEYNOTE 4** - WALLY RHINES (Mentor Graphics)			INDUSTRY FORUM
09.20 - 10.35 hrs	**Session A4:** Verification and Formal Methods	**Session B4:** Low-power Circuit Design	**Session C4:** SOI	
11.00 - 12.40 hrs	**Session A5:** Architectural Exploration and Design Closure	**Session B5:** Low-power Architecture	**Session C5:** Circuit Design and Modeling II	
13.40 - 14.25 hrs	**TECHNICAL KEYNOTE 5** - PRITH BANERJEE (HP Labs)			
14.30 - 16.10 hrs	**Session A6:** Design Challenges in Nano-CMOS	**Session B6:** Scheduling and Operating Systems	**Session C6:** Novel Circuit Design	Design, EDA & Systems Contest
16.30 - 18.00 hrs	**THEME SESSION:** AFFORDABLE TECHNOLOGIES FOR EMERGING MARKETS			
18.30 - 18.45 hrs	AWARDS DISTRIBUTION			
18.45 - 19.30 hrs	**BANQUET SPEECH** - AHMAD BAHAI (National Semiconductor)			

Thursday, 7 Jan 2010

09.00 - 09.45 hrs	**TECHNICAL KEYNOTE 7** - GREG TAYLOR (Intel)			EDUCATION FORUM
09.50 - 11.05 hrs	**Session A7:** Scan Testing	**Session B7:** Nanoelectronic Design	**Session C7:** Circuit Design I	
11.30 - 12.45 hrs	**Session A8:** Fault Models and Test Generation	**Session B8:** Secure / Reversible Computing	**Session C8:** Circuit Design II	
13.45 - 14.30 hrs	**TECHNICAL KEYNOTE 8** - YERVANT ZORIAN (Virage Logic)			
14.35 - 16.40 hrs	**Session A9:** Microfluidics and Fault Diagnosis	**Session B9:** 3D ICs and Network-on-chip	**Session C9:** System Design and IP Protection	
16.45 - 17.45 hrs	ISA / VSI / ACADEMIC PANEL			

VENUE LAYOUT - FIRST FLOOR

EMBEDDED TUTORIALS INFORMATION
Wednesday, 6 Jan 2010

14.30 - 15.15 hrs
AUDI 2

Track B / Embedded Tutorial 5: Front-end design flows for systems on chip

AUTHORS: **A. Kumar, P. Panda -** IIT Delhi

Description : This tutorial describes the design flows, that is, the design steps and software tools required for designing modern systemson-chip, focusing on the front end part. A simple flow starting with abstract design description in an HDL and going through transformations leading to physical design, is no longer adequate for the complex systems of today. A high end MPSoC (multiprocessor system on chip) today includes, apart from multiple processors, multiple memory modules, high performance interconnection network, custom hardware blocks, and a variety of controllers and interfaces. Some of the issues that need to be addressed while designing such systems are - integrated design of hardware and software, customization of processors for given applications in order to get the right power performance tradeoffs, use of certain platforms and predesigned IPs, design of interconnection mechanisms among the processors and mapping of application onto the architecture. Therefore, our description of design flow includes several 'subflows' that are required to take care of these aspects.

14.30 - 15.15 hrs
BOARD ROOM

Track C / Embedded Tutorial 6: FinFET SRAM design

AUTHORS: **R.Joshi, K. Kim, R. Kanj -** IBM

Description : This paper describes the SRAM design concept in FinFET technologies using unique features of non-planar double-gated devices. The parameter space required to design FinFETs is explored. Variety of SRAM design techniques are presented exploiting the advantages of tied gate and independent gate controlled configurations. SRAM performance, power, and stability for FinFET devices are compared with conventional planar CMOS counterparts. Modeling the variability of FinFETs through statistics is presented as well.

EMBEDDED TUTORIALS INFORMATION
Thursday, 7 Jan 2010

14.30 - 15.20 hrs
AUDI 3

Track A / Embedded Tutorial 7: Digital microfluidic biochips: A vision for functional diversity and more than Moore

AUTHOR: **K. Chakrabarty -** Duke University

Description : Microfluidics-based biochips are revolutionizing high throughput sequencing, parallel immunoassays, clinical diagnostics, and drug discovery. These devices enable the precise control of nanoliter volumes of biochemical samples and reagents. Compared to conventional laboratory procedures, which are cumbersome and expensive, miniaturized biochips offer the advantages of higher sensitivity, lower cost due to smaller sample and reagent volumes, system integration, and less likelihood of human error. This embedded tutorial paper provides an overview of droplet-based "digital" microfluidic biochips. It describes emerging computer-aided design (CAD) tools for the automated synthesis and optimization of biochips from bioassay protocols. Recent advances in fluidic-operation scheduling, module placement, droplet routing, pin-constrained chip design, and testing are presented.

14.30 - 15.20 hrs
BOARD ROOM

Track B/ Embedded Tutorial 8: Novel architecture deisgn with 3D integration technology

AUTHOR: **Y. Xie -** Penn State University

Description : The emerging three-dimensional (3D) chip architectures, with their intrinsic capability of reducing the wire length, is one of the promising solutions to mitigate the interconnect problem in modern microprocessor designs. 3D memory stacking also enables much higher memory bandwidth for future chip-multiprocessor design, mitigating the "memory wall" problem. In addition, heterogenous integration enabled by 3D technology can also result in innovation designs for future microprocessors. This paper serves as a survey of various approaches to design future 3D microprocessors, leveraging the benefits of fast latency, higher bandwidth, and heterogeneous integration capability that are offered by 3D technology.

14.30 - 15.20 hrs
AUDI 2

Track C/ Embedded Tutorial 9: Video coding tools and their impact on compression engine architecture

AUTHOR: **A. Rao -** Texas Instruments

Description : Video codec standards incorporate complex toolsets of algorithms that allow flexible trade-offs between end-application requirements such as compression efficiency, latency, power consumption and error resilience as well as implementation parameters such as power, cost and memory bandwidth. In this tutorial, we survey the most important video codec tools, the end-application scenarios they apply to, and their impact on the codec implementation architecture

PANEL SESSION
Tuesday, 5 Jan 2010

17.00 - 18.00 hrs

AUDI 1

Executive/CTO Panel: Is Open Source the Game Changer for Hardware Industry?

MODERATOR: Raman Santhanakrishnan - LSI Logic
PANELISTS: Guru Ganesan - ARM, Vikas Kohli - Cadence, Santosh Kumar - Texas Instruments, Prof. Rahul De - IIM Bangalore

Description : Open Source Software is all the rage in the computing world today. Competition in the software industry is intense, barriers have been broken, new players are emerging and more innovative products are brought to the market in shorter time. Clearly, open source movement has helped contribute a lot to these trends. Can a similar trend is possible in the hardware sector? When it comes to open source movement, EDA and IP markets have not seen much traction.

Why hasn't the open source movement succeeded yet in the hardware industry? Isn't there real value to be delivered to consumers via the open source route? What are the barriers to such a move? These are pertinent questions on our minds.

Proponents could argue that an open environment based on industry standards can lead to more innovation when a wider network of engineers across the world freely collaborate, unfettered by restrictions imposed by today's closed platforms. There has been a noteworthy success in the embedded world already. Well, in a crowded market already, margins are under tremendous pressure and the last thing companies want is to enable more players by embracing open source. And, what happens to innovation when there is no clear profit motive in an open source situation. And, what role can the India ecosystem play in such an outcome? Does the availability of a large pool of talent in India contribute to the growth of open source hardware?

Come and join this panel discussion and see the spirited debate by an illustrious panel comprising heads of R&D centers, academicians and technologists.

THEME SESSION
Wednesday, 6 Jan 2010

AUDI 1

16.30 - 17.00 hrs

Lecture 1: The Role of VLSI for SATCOM Applications

PRESENTER: **K. S. Dasgupta -** ISRO

Description : In this talk, I will cover the type of devices (FPGA) required for onboard applications and also type of devices required for ground systems - telemedicine and tele-education network for societal applications.

17.00 - 17.30 hrs

Lecture 2: From Accessible Technologies to Affordable Solutions

PRESENTER: **Sham Banerji -** i2i TeleSolutions

Description : Customer solutions for emerging markets creates unique affordability challenges that sometimes require the latest technologies to be deployed in unusual and innovative ways to make them scalable and available on a wide scale.

The presentation covers examples of such innovation and deployment in the area of Telemedicine for Healthcare.

17.30 - 18.00 hrs

Lecture 3: Designing Technologies for the Rural Context

PRESENTER: **William Thies -** Microsoft Research India

Description : Many technologies that we take for granted remain inaccessible or inappropriate for rural communities, due to barriers such as cost, usability, and robustness. In the Technologies for Emerging Markets Group at Microsoft Research India, we seek to invent and apply technologies that are specifically tailored to foster socio-economic development, spanning diverse sectors such as education, agriculture, microfinance, and healthcare. This talk will focus on the domain of healthcare, where our research ranges from high-tech (developing the software underpinnings to enable versatile lab-on-a-chip diagnostic systems) to low-tech (utilizing commodity biometrics to improve the delivery of tuberculosis medications). While high-tech innovations promise benefits in the long-term, we believe that much of the opportunity lies in finding creative applications, adaptations, or extensions of existing technologies to suit the needs of organizations working in rural communities.

TECHNICAL PROGRAM
Tuesday, 5 Jan 2010

7.30 AM - 8.45 hrs
Conference Registration

8.45 - 11.00 hrs
AUDI 1 PLENARY SESSION

Conference Inauguration
Dr. Biswadip Mitra - President, VSI & Managing Director - Texas Instruments India

General and Program Chairs Addresses

TECHNICAL KEYNOTES 1 & 2:
Chair: Niraj K. Jha - Princeton University

Nanoelectronics challenges for the 21st century
Prof. Dimitri Antoniadis, Director, MIT

Deep Submicron CMOS Technology – the challenges for semiconductor IDM
Prof. Dr. Hermann Eul, Group VP & GM, Infineon

11.00 - 11.30 hrs BREAK

11.30 - 12.45 hrs

BOARD ROOM **SESSION A1: Clocking and Physical Design**
Chair: Bharadwaj Amrutur - IISc Bangalore

A1.1: *Analysis, Design and Simulation of Capacitive Load Balanced Rotary Oscillatory Array.*
V.Honkote, B.Taskin - Drexel University

A1.2: *Introduction of an Alternative Approach to Buffer Insertion for Delay and Power Reduction in VLSI Interconnects*
S. Saini, A. M. Kumar, S. Veeramachaneni - IIIT Hyderabad, M. B. Srinivas - BITS Hyderabad

A1.3: *A Graph-based I/O Pad Pre-placement Technique for use with Analytic FPGA Placement Methods.*
G.Grewal, M.Xu - University of Guelph, Ontario

11.30 - 12.45 hrs

AUDI 1 **SESSION B1: Application-specific Architectures**
Chair: Debdeep Mukhopadhyay - IIT Kharagpur.

B1.1: *Instruction selection in ASIP Synthesis using functional matching.*
N.Arora - One97 Communications, A.Kumar - IIT Delhi, K.Chandramohan - Synfora, N. Pothineni - Google

β B1.2: *A 90mW / GFlop 3.4GHz Reconfigurable Fused/Continuous Multiply-Accumulator for Floating-point and Integer Operands in 65nm.*
S.Jain, V.Erraguntla, S.Vangal, Y.Hoskote, N.Borkar, T.Mandepudi, Karthik V.P. - Intel

B1.3: A Reconfigurable Architecture for Secure Multimedia Delivery.
A.Pande, J.Zambreno - Iowa State University, Ames

β - Best Paper Nominee

TECHNICAL PROGRAM
Tuesday, 5 Jan 2010

11.30 - 12.45 hrs

AUDI 2 **SESSION C1: High-speed Links**
Chair: Pradip Thaker - Analog Devices

C1.1: *Channel Optimization for the Design of High Speed I/O links.*
R. Mandrekar, Y. Zhou, S. Chun, A. Haridass, J. Choi, N. Na, D. Dreps, R. Weekly, P. Harvey - IBM

C1.2: *High Speed Serial Link Transmitter for 10Gig Ethernet Applications.*
V. Muniyappa, N. Ramamoorthy, J. Reddy - IBM

C1.3: *Architectural Comparison of Analog and Digital Duty Cycle Corrector for High Speed I/O Link.*
L. Raghavan, T. Wu - Rambus

12.45 PM - 13.45 hrs LUNCH

13.45 - 14.30 hrs

AUDI 1 **TECHNICAL KEYNOTE 3:**
Chair: C. P. Ravikumar - Texas Instruments

DLP® technology: Extreme Versatility
Larry Hornbeck - Texas Instruments

14.35 - 15.50 hrs

BOARD ROOM **SESSION A2: Analog / RF CAD**
Chair: Jaggy Rao - Texas Instruments.

A2.1: *An Improvised MOS Transistor Model Suitable for Geometric Program based Analog Circuit Sizing in Sub-micron Technology.*
S.Dasgupta, P.Mandal - IIT Kharagpur

A2.2: *Towards Active-Passive Co-Synthesis of Multi-GigaHertz Radio Frequency Circuits.*
R.Chakraborty, A.Sathanur, V.Jandhyala - University of Washington, Seattle

A2.3: *An Efficient Method for Bottom-Up Extraction of Analog Behavioral Model Parameters.*
S. Pam, A. Bhattacharya, S. Mukhopadhyay - IIT Kharagpur

14.35 - 15.50 hrs

AUDI 1 **SESSION B2: Efficient System Modeling and Design**
Chair: Kanishka Lahiri, AMD.

β B2.1: *Bottleneck Identification Techniques Leading to SimplifiedPerformance Models for Efficient Design Space Exploration in VLSI Memory Systems.*
G. Hazari, M. Desai, G. Srinivas - IIT Mumbai

B2.2: *Implementation of a Novel Phoneme Recognition System using TMS320C6713 DSP.*
J. Manikandan, B. Venkataramani, M.Bhaskar, K. Ashish, R. Raghul, V.Mathangi - NIT Trichy

β - Best Paper Nominee

B2.3: *Design of Low-Cost High-performance Floating-point Fused Multiply-Add with Reduced Power.*
Z. Qi, Q. Guo, X. Li, G. Zhang, W. Hu - Chinese Academy of Sciences

14.35 - 15.50 hrs

AUDI 2 **SESSION C2: Circuit Design and Modeling I**
Chair: Kota Murali - IBM

C2.1: *On Electrical Modeling of Imperfect Diffusion.*
T.B. Chan, P. Gupta - University of California, Los Angeles

C2.2: *An L-band Fractional-N Synthesizer with Noise-less Active Capacitor Scaling.*
D. Sahu, S. Ganeshan, A. Lachhwani, R. Sachdev, Chandrashekar B.G - Texas Instruments

C2.3: *On-Chip Inductor-less DC-DC Boost Converter with Non-Overlapped Rotational-Interleaving Scheme.*
T.Das, P.Mandal - IIT Kharagpur

15.50 - 16.10 hrs BREAK

16.10 - 16.55 hrs

BOARD ROOM **SESSION A3: Tackling Process Variations**
Chair: TBD

A3.1 / ET1: Embedded Tutorial: *Electrical Modeling of Imperfect Lithographic Patterning*
T.B. Chan, R. Ghaida, P. Gupta - University of California, Los Angeles

16.10 - 16.55 hrs

AUDI 1 **SESSION B3:** *Robust Design*
Chair: M.Balakrishnan - IIT Delhi

B3.1 / ET2: Embedded Tutorial: *Robust System Design*
S.Mitra - Stanford University

16.10 - 16.55 hrs

AUDI 2 **SESSION C3: Chip 2020**
Chair: Sur-Kolay - ISI Kolkata

C3.1 / ET3: Embedded Tutorial: *Chip of 2020: Designing Low-Cost Energy-Efficient Complex Systems using Heterogeneous Components.*
K.Roy, B.Jung, A.Raghunathan - Purdue University

17.00 - 18.00 hrs

AUDI 1

Executive/CTO Panel: *Is Open Source the Game Changer for Hardware Industry?*

Moderator: Raman Santhanakrishnan - LSI Logic
Panelists: Guru Ganesan - ARM, Vikas Kohli - Cadence, Santosh Kumar - Texas Instruments, Prof. Rahul De - IIM Banaglore

TECHNICAL PROGRAM
Wednesday, 6 Jan 2010

08.30 - 09.15 hrs

AUDI 1 **TECHNICAL KEYNOTE 4:**
Chair: Vasantha Erraguntla - Intel

Delivering 10X Design Improvements
Dr. Walden C. Rhines - CEO, Mentor Graphics

09.20 - 10.35 hrs

AUDI 1 **SESSION A4: Verification and Formal Methods**
Chair: Kaushik De - Synopsys

A4.1: *Synthesizability of Three Party Formal Specifications - Does My controller See Enough?*
A. Banerjee - Interra Systems

β A4.2: *Coverage Management with Inline Assertions and Formal Test Points*
A. Hazra, P. Ghosh, P. Dasgupta, P. Chakrabarti - IIT Kharagpur

A4.3: *Synchronized Generation of Directed Tests Using Satisfiability Solving*
X. Qin, M. Chen, P. Mishra - University of Florida, Gainesville

09.20 - 10.35 hrs

AUDI 2 **SESSION B4: Low-power Circuit Design**
Nachiket Urdhwareshe - Softjin

B4.1: *A Combined DOE-ILP Based Power and Read Stability Optimization in Nano-CMOS SRAM*
G. Thakral, S. Mohanty, D. Ghai - University of North Texas, D. Pradhan - University of Bristol

B4.2: *Novel Vth Hopping Techniques for Aggressive Runtime Leakage Control*
H.Xu, W-B.Jone, R.Vemuri - University of Cincinnati

B4.3: I*nexact Decision Circuits: An Application to Hamming Weight Threshold Voting*
B. Rajaram, A. Ramachandran, S. Purini, G. Regeti - IIIT Hyderabad

09.20 - 10.35 hrs

BOARD ROOM **SESSION C4: SOI**
Chair: Santanu Mahapatra - IISc Bangalore

C4.1: *RF SOI Switch FET Design and Modeling Tradeoffs for GSM Applications*
S.Parthasarathy, Y.Chauhan, A.Trivedi, M.Olsen, R.Groves, S.Sirohi - IBM

C4.2: *Modeling of High Frequency Noise in SOI*
M. Varadharajaperumal, S. Sirohi, S. Khandelwal, V. Subramanian, T. Ethirajan - IBM

C4.3: *A New Hetero-material Stepped Gate SOI LDMOS for RF Power Amplifier Applications*
R. Sithanandam, M.J. Kumar - IIT Delhi

10.35 AM - 11.00 AM BREAK

β - Best Paper Nominee

TECHNICAL PROGRAM
Wednesday, 6 Jan 2010

11.00 - 12.40 hrs

AUDI 1

SESSION A5: Architectural Exploration and Design Closure
Chair: TBD

A5.1: *A Methodology for Power Aware High-Level Synthesis of Co-Processors from Software Algorithms*
S. Ahuja, S. Shukla, A. Lakshminarayana - Virginia Tech, Blacksburg, W.Zhang - Cebatech

A5.2: *A Hierarchical Methodology for Word-Length Optimization of Signal Processing Systems*
K. Parashar, R. Rocher, D. Menard, O. Sentieys - University of Rennes-1, Lannion

A5.3: *Post-assembly Timing Closure for Multi-million Gate Chips*
S. Prasad, O. Levitsky, D. Liu, S. Srivastava, K.L. Cheong, D. Noice - Cadence Design Systems

A5.4: *Accelerating Synchronous Sequential Circuits Using an Adaptive Clock*
A.Mondal - Berkeley Design Automation, P. Chakrabarti, P. Dasgupta - IIT Kharagpur

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11.00 - 12.40 hrs

AUDI 2

SESSION B5: Low-power Architecture
Chair: Saraju Mohanty - University of North Texas

B5.1: *Voltage-Frequency Planning for Thermal- \Aware, Low Power Design of Regular 3D NoCs*
M. Arjomand, H. Sarbazi-Azad - Sharif University of Technology, Tehran

B5.2: *Leakage-Aware Energy Minimization Using Dynamic Voltage Scaling and Cache Reconfiguration in Real-Time Systems*
W. Wang, P. Mishra - University of Florida, Gainesville

β B5.3: *Rethinking Threshold Voltage Assignment in 3D Multicore Designs*
K. Chakraborty, S. Roy - Utah State University

B5.4: *Transition Inversion based Low Power Data Coding Scheme for Buffered Data Transfer*
A. Ramachandran, B. Rajaram, S. Purini, G. Regeti - IIIT Hyderabad

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11.00 - 12.40 hrs

BOARD ROOM

SESSION C5: Circuit Design and Modeling II
Chair: Swarup Bhunia - Case Western University

C5.1: *Design Considerations for BEOL MIM Capacitor Modeling in RF CMOS Process.*
B. Swaminathan, S. Parthasarathy, A. Sundaram, R. Groves - IBM

β - Best Paper Nominee

C5.2: *Modeling of RF-MEMS BAW Resonator*
A. Roy, K. Prasad - University of Massachusetts Lowell, B. Barber - Skyworks Solutions

C5.3: *High Speed Clock and Data Recovery Circuit with Novel Jitter Reduction Technique*
K. Desai, V. Krishna, V. Khawshe, P. Venkatesan, R. Palwai, R. Nagulapalli - Rambus

C5.4: *A 6 bit 800MHz TIADC based on Successive Approximation in 65 mm Standard CMOS Process*
A. Salimath, S.K. Mandal - DAIICT, C. Debnath, K. Chatterjee - ST Microelectronics,

12.40 - 13.40 hrs LUNCH

13.40 - 14.25 hrs

AUDI 1 **TECHNICAL KEYNOTE 5:**
Chair: Anand Raghunathan - Purdue University

Future Research Directions in Electronic Design Automation
Dr. Prith Banerjee - Director , HP Labs

14.30 - 16.10 hrs

AUDI 1 **SESSION A6: Design Challenges in Nano-CMOS**
Chair: V.Vishwanathan - Texas Instruments

A6.1 / ET4: Embedded Tutorial: *The New World Order at the Dawn of 22nm Era!*
R.Puri - IBM

A6.2: *A P4VT (Power-Performance-Process- Parasitic-Voltage-Temperature) Aware Dual-VTh Nano-CMOS VCO*
S.Mohanty, D.Ghai, E.Kougianos - University of North Texas

A6.3: *Optical Lithography Simulation with focus Variation Using Wavelet Transform*
R.Rodrigues, S.Kundu - University of Massachusetts, Amherst

14.30 - 16.10 hrs

AUDI 2 **SESSION B6: Scheduling and Operating Systems**
Chair: Sanjiv Narayan - Calypto Systems

B6.1 / ET5: Embedded Tutorial: *Front-End Design Flows for Systems on Chip*
A. Kumar, P. Panda - IIT Delhi

B6.2: *A Hardware Scheduler for Real Time Multiprocessor System on Chip*
N. Gupta, S. Mandal, J. Malave, A. Mandal, R. Mahapatra - Texas A & M University

B6.3: *Safe-ERfair - A priori Overload Handling in Fair Scheduled Embedded Systems*
A. Sarkar, R. Nanda, S. Ghose, P. Chakrabarti - IIT Kharagpur

TECHNICAL PROGRAM
Wednesday, 6 Jan 2010

14.30 - 16.10 hrs

BOARD ROOM **SESSION C6: Novel Circuit Design**
Chair: Dinesh Sharma, IIT Mumbai.

C6.1 / ET6: Embedded Tutorial: *FinFET SRAM Design*
R. Joshi, K. Km, R. Kanj - IBM

C6.2: *A Non Quasi-Static Small Signal Model for Long Channel Symmetric DG MOSFET*
S. Sarkar, S. Mahapatra - IISc Bangalore, A. Roy - Intel

C6.3: *A Novel Circuit to Optimize CLK-WL Path and Decoding Schemes in Memories*
S. Jain, K. Srivastva, S. Kainth - Virage Logic

16.10 - 16.30 hrs BREAK

16.30 - 18.00 hrs

AUDI 1 **THEME SESSION: Affordable Technologies for Emerging Markets**
Chair: Srivaths Ravi - Texas Instruments

Lecture 1: *The Role of VLSI for SATCOM Applications*
K. S. Dasgupta, ISRO

Lecture 2: *From Accessible Technologies to Affordable Solutions*
Sham Banerji - i2i TeleSolutions

Lecture 3: *Designing Technologies for the Rural Context*
William Thies - Microsoft Research India

18.00 - 18.30 hrs BREAK

18.30 - 19.30 hrs

AUDI 1 **AWARDS DISTRIBUTION**

BANQUET SESSION:
Chair: Srimat Chakradhar - NEC

Green Energy - Emerging Technologies and their impact in better energy efficiency realization
Dr. Ahmad Bahai, CTO, Fellow and Director of Research Labs at National Semiconductor

19.30 - 20.30 hrs DINNER

TECHNICAL PROGRAM
Thursday, 7 Jan 2010

09.00 - 09.45 hrs

AUDI 1 **TECHNICAL KEYNOTE 7:**
Chair: Navakant Bhat - IISc Bangalore

Future of Analog Design and Upcoming Challenges in Nanometer CMOS
Dr. Gregory F. Taylor - Fellow, Intel

09.50 - 11.05 hrs

AUDI 3 **SESSION A7: Scan Testing**
Chair: Erik Larsson - Linkoping University

A7.1: *A Unified Solution to Scan Test Volume, Time, and Power Minimization*
S. Seth - University of Nebraska-Lincoln, Z. Chen, D. Xiang - Tsinghua University, B. Bhattachary - ISI Kolkata.

A7.2: *Hamming Distance Based Reordering and Column-wise Bit Stuffing with Difference Vector: A Better Scheme for Test Data Compression with Run Length Based Code*
U. Mehta, N. Devashrayee - Nirma University, K. Dasgupta - ISRO.

A7.3: *On Minimization of Test Aplication Time for RAS*
R. Adiga, A. Gandhi, V. Singh - IISC Bangalore, K. Saluja - University of Wisconsin-Madison, H. Fujiwara - Nara Institute of Science and Technology, A. Singh - Auburn University.

09.50 - 11.05 hrs

BOARD ROOM **SESSION B7: Nanoelectronic Design**
Chair: Bernard Courtois - CNRS Grenoble

B7.1: *Identifying the Bottlenecks to the RF performance of FinFETs*
V. Subramanian - IBM, B. Parvais, A. Mercha, M. Dehan, G. Groeseneken, S.Decoutere - IMEC, Leuven, W. Sansen - KU Leuven

B7.2: *Analyzing Energy-Delay Behavior in Room Temperature Single Electron Transistors*
V. Saripalli, V. Narayanan, S. Datta - Penn State University

B7.3: *Clocking-based Coplanar Wire Crossing Scheme for QCA*
R. Devadoss, K. Paul, M. Balakrishnan - IIT Delhi

09.50 - 11.05 hrs

AUDI 2 **SESSION C7: Circuit Design I**
Chair: Prakash Easwaran - Cosmic Circuits

C7.1: *Optimized Stage Ratio of Tapered CMOS Inverters for Minimum Power and Low Mismatch Jitter Product*
R. Dutta, T. K Bhattacharyya - IIT Kharagpur, X. Gao, E. A. M. Klumperink - University of Twente

C7.2: *23.97GHz CMOS Distributed Voltage Controlled Oscillators with Inverter Gain and Frequency Tuning by Body Bias and MOS Varactors*
K.Bhattacharyya - IIT Mumbai

C7.3: *Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs*
H. Thapliyal, N. Ranganathan - University of South Florida, Tampa

11.05 - 11.30 hrs BREAK

11.30 - 12.45 hrs

AUDI 3 **SESSION A8: Fault Models and Test Generation**
Chair: Nagesh Tamarapalli - AMD

A8.1: *Identifying Tests for Logic Fault Models Involving Subsets of Lines Without Fault Enumeration*
I. Pomeranz - Purdue University, S. Reddy - University of Iowa

A8.2: *Impact of Temperature on Test Quality*
L. Jagan - IIT Chennai, C.Hora, B.Kruseman, S.Eichenberger, A.Majhi - NXP Semiconductors, V. Kamakoti - IIT Chennai

A8.3: *Test Pattern Generation and Compaction for Crosstalk Induced Glitches and Delay Faults*
S. Hasan, A. Palit, W. Anheier - University of Bremen

11.30 - 12.45 hrs

BOARD ROOM **SESSION B8: Secure / Reversible Computing**
Chair: Vijaykrishnan Narayanan - Penn State University

B8.1: *RTL Hardware IP Protection Using Key-Based Control and Data Flow Obfuscation*
R.Chakraborty, S.Bhunia - Case Western Reserve University

B8.2: *Pinpointing Cache Timing Attacks on AES*
C.Rebeiro, M.Mondal, D.Mukhopadhyay - IIT Kharagpur

B8.3: *An Efficient Design of a Reversible Barrel Shifter*
I. Hashmi - George Mason University, Virginia, H.H. Babu - University of Dhaka

11.30 - 12.45 hrs

AUDI 2 **SESSION C8: Circuit Design II**
Chair: Jagadesh Kumar - IIT Delhi

C8.1: *4 GHz 130nm Low Voltage PLL Based On Self Biased Technique*
V. Viswam, B. Viswanathan, Kulanthaivelu R., J. Vettickatt, R. Nair, L.Chandran - Network Systems and Technologies

C8.2: *An Improved High Resolution CMOS Timing Generator Using Array of Digital Delay Lock Loops*
S. Balaji - Anna University, Chennai, V.B. Chandratare - BARC, Mumbai

C8.3: *Analog Circuit Design Methodologies to Improve Negative-Bias Temperature Instability Degradation*
A.Ghosh, Ann Arbor, R.Brown - University of Utah, R.Franklin - University of Michigan

12.45 - 13.45 hrs LUNCH

13.45 - 14.30 hrs

AUDI 1 **TECHNICAL KEYNOTE 8:**
Chair: Ram Jonnavithula - Texas Instruments

Managing IP for SOCs at Advanced Process Nodes
Dr. Yervant Zorian - Vice President & Chief Scientist, Virage Logic

14.35 - 16.40 hrs

AUDI 3 **SESSION A9: Microfluidics and Fault Diagnosis**
Chair: Adit Singh, Auburn University

A9.1 / ET7: Embedded Tutorial: *Digital Microfluidic Biochips: A Vision for Functional Diversity and More than Moore*
K. Chakrabarty - Duke University

β A9.2: *Synchronization of Concurrently-Implemented Fluidic Operations in Pin-Constrained Digital Microfluidic Biochips*
Y. Zhao, K. Chakrabarty - Duke University, R. Sturmer, V. Pamula - Advanced Liquid Logic

A9.3: *Output-Dependent Diagnostic Test Generation*
I. Pomeranz - Purdue University, S. Reddy - University of Iowa

A9.4: *Parametric Fault Diagnosis of Nonlinear Analog Circuits Using Polynomial Coefficients*
S. Sindia - Analog Devices, V. Singh - IISc Bangalore,
V. Agrawal - Auburn University

14.35 - 16.40 hrs

BOARD ROOM **SESSION B9: 3D ICs and Network-on-chip**
Chair: Anshul Kumar - IIT Delhi

B9.1 / ET8: Embedded Tutorial: *Novel Architecture Design with Three-dimensional (3D) Integration Technology*
Y. Xie - Penn State University

B9.2: *Exploring Use of NoC for Reconfigurable Video Coding*
A. Patel - Cisco, H. Kapoor - IIT Guwahati

B9.3: *Design of NoC for SoC with Multiple Use Cases Requiring Guaranteed Performance*
G. Leary, K. Chatha - Arizona State University

β - Best Paper Nominee

14.35 - 16.40 hrs

AUDI 2

SESSION C9: System Design and IP Protection
Chair: V. Kamakoti - IIT Chennai

C9.1/ET9: Embedded Tutorial: *Video Coding Tools and Their Impact on Compression Engine Architecture*
A. Rao - Texas Instruments

C9.2: *Functional Refinement: A Generic Methodology for Managing ESL Abstractions*
A. Thimmapuram, S. Abrar - NXP Semiconductors

C9.3: *A Unified Approach for IP Protection across Design Phases in a Packaged Chip*
D. Saha, S. Sur-Kolay - ISI Kolkata

INDUSTRY FORUM PROGRAM
Tuesday, 5 Jan 2010

The Industry Forum (IF) track in VLSI 2010 is designed to facilitate interactions amongst the industry players specifically working on the theme of the conference; namely **"Affordable technology for emerging markets"**. This track is spread over the first two days of the main conference, January 5 & 6, 2010 and will feature a combination of individual company presentations, invited talks by industry experts and informative panel sessions on current state in technology and markets.

The IF track this year runs as follows:

VENUE: AUDI 3

SESSION IE: KICKOFF	
11.30 - 11.35 hrs	Inauguration
11.35 - 12.20 hrs	S1: Cisco-Webex
12.20 - 12.40 hrs	S2: Infineon
12.45 - 13.45 hrs	**LUNCH BREAK**
13.45 - 14.30 hrs	CONFERENCE PLENARY
SESSION 2E: DESIGN	
14.35 - 14.55 hrs	S3: Marvell
14.55 - 15.15 hrs	S4: Texas Instruments
15.15 - 16.15 hrs*	**IF PANEL 1:** *Emerging Product/Technologies: ex: Leapfrogging the technologies: Paper to UID; NanotoEnano; IncadLight to LED;* Moderator: Prof. Sadagopan, IIITB; Panelists: Rambus, KPITCummins, Agilient
16.15 - 16.45 hrs	IF - INVITED TALK 1 (Intel)

** Tea break included within the session*

INDUSTRY FORUM PROGRAM
Wednesday, 6 Jan 2010

VENUE: AUDI 3

SESSION 3E: EDA	
09.20 - 09.40 hrs	S5: Mentor
09.40 - 10.00 hrs	S6: Cadence
10.00 - 10.20 hrs	S7: Synopsys
10.20 - 10.40 hrs	Q & A
10.40 - 11.00 hrs	**BREAK**
SESSION 4E: IP	
11.00 - 11.20 hrs	S8: ARM
11.20 - 11.40 hrs	S9: Rambus
11.40 - 12.40 hrs	**IF PANEL 2:** *Emerging Markets: How are new methodologies, technologies enabling emerging markets to play larger role* Moderator: Dr. Mahesh Mehendale, TI Panelists: Mentor, Xilinx, M3
12.40 - 13.40 hrs	**LUNCH BREAK**
13.40 - 14.25 hrs	CONFERENCE PLENARY
SESSION 5E: DESIGN	
14.30 - 14.50 hrs	S10: Intel
14.50 - 15.10 hrs	S11: Lantiq
15.10 - 15.30 hrs	S12: LSI
15.30 - 15.40 hrs	Q & A
15.40 - 16.10 hrs	IF - INVITED TALK 2 (TI)

For details, please contact:

Vikas Gautam, Exhibits Chair, vikas.gautam@synopsys.com
S. Uma Mahesh, Sponsorship Chair, sum_mahesh@yahoo.co.in
Dr. Pradip K. Dutta, Industry Forum Chair, pradip.dutta@synopsys.com

DESIGN, EDA AND SYSTEMS CONTEST
Thursday, 7 Jan 2010

This year, four entries have been chosen for the finals of the **Design/EDA/Systems design contest**. The final presentations will be on the afternoon of 5th Jan. 2010 between 2:35pm and 4:55pm *(in parallel with the last two paper sessions on the first day of the conference)*. Please check for contest room location at the information desk.

Selected entries for the finals:

- *Fixing Hold In Shift Mode Without Adding Buffers*
  Sachin Mathur, Shalini Miyan - ST Microelectronics, Greater Noida

- *Quick and Effective way to verify customer appliation use cases of a SoC wrt Power Management*
  Vinay Amancha - Texas Instruments, Bangalore

- *Design Automation For Implementation Of A Parallel Architecture For LDPC Decoder*
  Vikram Chandrasetty - University of South Australia

- *Low Power, Low Cost RFID Tag Reader*
  Ankur Gandhe, Sarabjot Singh, Roy Paily - IIT Guwahati

EDUCATION FORUM PROGRAM
Thursday, 7 Jan 2010

VLSI Conference 2010 introduces an **"Education Forum"** program, with a series of lectures on current topics of research and state-of-the-art techniques. These lectures are given by leaders from industry/academia within the framework of the VLSI conference. The intent of this forum is to provide an opportunity to faculty members of engineering studies and to the students and fresh engineers in relevant disciplines of engineering to hear on advanced research areas in VLSI engineering. The registrants would get a certificate of participation in this forum.

The Workshop:
The 1-day workshop will be delivered by experts from renowned Industries and world class universities. The agenda for the day-long programme is noted below.

VENUE : AUDI 1

08.00 - 08.45 hrs	Registration/Logistics
09.00 - 09.45 hrs	**Technical Keynote 6 - *(Venue Audi 1)*** Greg Taylor - Intel
09.50 - 10.20 hrs	*Perspectives on VLSI Education* Dr.Chandrasekhar - CEERI
10.20 - 11.00 hrs	*Digital VLSI design/test* Prof.Saluja - Univ. Wisconsin-Madison
11.05 - 11.25 hrs	**BREAK**
11.25 - 12.05 hrs	*A Network Synthesis based approach towards understanding Analog IC design* Dr.KRK Rao - Texas Instruments
12.05 - 12.45 hrs	*Low-power CMOS design* Prof.Vishwani Agrawal, Auburn Univ
12.45 - 13.45 hrs	**LUNCH BREAK**
13.45 - 14.30 hrs	**Technical Keynote 7 - *(Venue Audi 1)*** Yervant Zorian - Virage Logic
14.35 - 15.15 hrs	*Techniques assuring logical correctness of hardware design* Prof. M. Fujita - Univ. Tokyo
15.15 - 15.55 hrs	*Software influenced silicon architectures for embedded systems* Vasant Easwaran - Texas Instruments
15.55 - 16.25 hrs	**BREAK**
16.25 - 17.05 hrs	*Semiconductor Packaging: Introduction, Challenges and Trends* Dr.Arun Chandrasekhar - Intel
17.05 - 17.45 hrs	*Nanowire electronics and applications* Prof. Jagadesh - IITD

EDUCATION FORUM PROGRAM
Thursday, 7 Jan 2010

Eligibility: Faculty members in Electronics / Electrical / Communications / Computers / Instrumentation / Information Technology and other allied fields, and students doing B.Tech / B.E / MSc / M.Tech / M.E in these areas. Professionals starting their careers in the semiconductor industry are also welcome to attend.

Enrollment: Online Registration Click Here

Required document to be presented at the venue:ID card from the parent institution

Contacts: The contact details for the chairs of this programme are noted below:

Dr.Virendra Singh (virendra @computer.org)
R.Venkatraman (rvenkat@ti.com)

REGISTRATION AND VIDEO CONFERENCING

Admission to VLSID 2010

A personal registration badge is required for admission into the conference Premises. In the interest of personal security, all participants are expected to wear the badge at all times in the conference venue. Badge will be delivered to participants at the time of registration at the conference venue. Participants are expected to carry personal photo identity card to authenticate their identity at the time of registration. Participants who have availed member rates will be expected to preset their card at the time of registration.

Personal Safety

Visitors to any city should take steps to reduce their vunerability to crime. Walk with others, especially at night. Check with your hotel information desk before visiting any unfamiliar places. Use services from authorized agencies only. Share your identity on a need-to-know basis. Keep your personal belongings in safe custody. Your conference badge is non-transferable and for your personal use only, treat it that way. Do not share your badge with others.

Smoking

Smoking is prohibited in the entire conference facility at all times. Carrying Cigarettes, Lighters, Match boxes and other inflammable items is prohibited.

Parking

Parking is limited in the conference facility, Participants are requested to explore CarPool options as a first choice.

"Conference-on-Desktop" Option

VLSID 2010 is available on desktop for people who are unable to attend the conference in person. One way video & audio streaming live to your desktop/Laptop with Cisco Webex.

Streaming Schedule

Tuesday, 5th Jan 2010	**Track B, Track C, Industry Forum**
Wednesday, 6th Jan 2010	**Track A, Track B, Industry Forum**
Thursday, 7th Jan 2010	**Track A, Track C, Education Forum**

System Requirements

Broadband connectivity with minimum 256Kbps speed, multimedia speakers on your Desktop.

Onsite Registration Hours

Tutorials:

Sunday, 3rd Jan 2010	8:00 AM - 1:00 PM
Monday, 4th Jan 2010	8:00 AM - 1:00 PM

Conference/Exhibitors:

Tuesday. 5th Jan 2010	7:30 AM - 1:00 PM
Wednesday, 6th Jan 2010	7:30 AM - 1:00 PM
Thursday, 7th Jan 2010	8:00 AM - 1:00 PM

Education Forum:

Thursday, 7th Jan 2010	8:00 AM - 1:00 PM

REGISTRATION AND VIDEO CONFERENCING

REGISTRATION CHARGES

Registration options – Charges listed are in INR.				
	Early Bird (Till 07Dec2009)		Regular (From 08Dec2009)	
	Members*	Non-Members	Members*	Non-Members
Conference	Rs. 6000	Rs. 6500	Rs. 7500	Rs. 8000
1-day Tutorial	Rs. 2250	Rs. 2500	Rs. 3250	Rs. 3500
2-day Tutorial	Rs. 4000	Rs. 4500	Rs. 6000	Rs. 6500
Education Forum	NA		Rs. 800	
Webex Conferencing	NA		Rs. 2500	

* Member refers to Individuals having membership or affiliation to IEEE, ACM or VSI. Members are expected to Produce the membership cards at the time of registration.

- Education Forum is targeted towards, Under graduate and Post Graduate Engineering Students, Faculty Members, Graduates passed out in the recent acedemic year.
- Webex conferencing is being introduced for 2 tracks and Industry forum with an effort to enable participation from people who have not been able to travel to Bangalore for various reasons,
- Online Registrations can be done using Credit cards or DD addressed to " VSI – VLSI DESIGN 2010 " payable at Bangalore.
- Rates in the regular column apply to On-site registration. Payment can be done in Cash or VIA a DD.
- Photo Identity proof to Validate personal identity is mandatory for registrations that require physical presence in the Venue.

VENUE INFORMATION

VENUE :
NIMHANS CONVENTION CENTRE
Hosur Road, Near Lakkasandra Bus Stop
Bangalore - 560 029

TUTORIAL 8 VENUE:
Synopsys (I) Pvt. Ltd.
RMZ Infinity, Tower A , 3rd,4th and 5th Floor,
Muncipal #3, Benniganahalli
Old Madras Road
Bangalore, India 560016

EXHIBITORS INFORMATION

VLSID 2010's exhibits program has an exciting array of over 26 exhibitors that include industry players from across semiconductor design, electronic design automation, IP reuse, design services and consulting and representation from couple of institutes popularizing VLSI education in India. The three-day program runs concurrently with the technical program, and will provide an opportunity to interact with the following exhibitors:

Agilent
Aldec
Arasan Chip Systems
ARM
Bluespec
CMRDA
Cypress Semiconductor
D'gipro
eInfochips
ESDS
EVE Design Automation
Icon Design Automation
Infineon Technologies
Intrinsic
KPIT-Cummins
nSys Design Systems
QThink IC Design
Rambus
RV-VLSI
Sankhya Technologies
Seer Akademi
Synopsys
Trident Techlabs
Whizchip Design Technologies
Wipro Technologies
Xilinx

Exhibit hours:
Jan 5 : 11:00 hrs to 18:30 hrs
Jan 6 : 09:30 hrs to 18:30 hrs
Jan 7 : 09:30 hrs to 17:00 hrs

RASDAT WORKSHOP

IEEE International Workshop on Reliability Aware System Design and Test
RASDAT 2010, *IISc, Bangalore, January 7-8, 2010*

Scope: Even as advances in CMOS technology come up against physical limits of material properties and lithography, raising many new challenges that must be overcome to ensure IC quality and reliability, there appears to be no obvious alternate technology that can replace end-of-roadmap CMOS over the next decade. However, many reliability challenges from increasing defect rates, manufacturing variations, soft errors, wear-out, etc,. will need to be addressed by innovative design and test methodologies if device scaling is to continue on track as per Moore's Law to 10nm and beyond. The key objective of this annual workshop, planned to be held in conjunction with the International Conference on VLSI Design, is to provide an informal forum for vigorous creative discussion and debate of this area. The aim is to encourage the presentation and discussion of truly innovative and "out-of-the-box" ideas to address these challenges that may not yet have been fully developed for presentation at reviewed conferences.

The workshop program includes a keynote address (Yervant Zorian), a banquet speech (Greg Taylor) several invited talks(Mark Zwolinski, Bernd Becker, Shubu Mukherjee), an embedded tutorial (Abhijit Chatterjee), twelve regular presentations, and a panel discussion on "End of CMOS Roadmap – Test and Reliability Challenges".

The research topics include:

- Design for test
- Built-in self-test
- ATPG and defect oriented test
- Delay test
- Low power test
- Instruction-based self-test
- On-line test methodology
- Reliability of CMOS circuits
- Self-checking circuits
- Self-diagnosis methods
- Fault tolerant micro-architecture
- Self-healing system design
- Energy and performance aware
- Fault-tolerant micro-architectures
- Device degradation and mitigation
- System validation methodology
- Secure system design
- Design for reliability and dependability
- Design for or verifiability

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